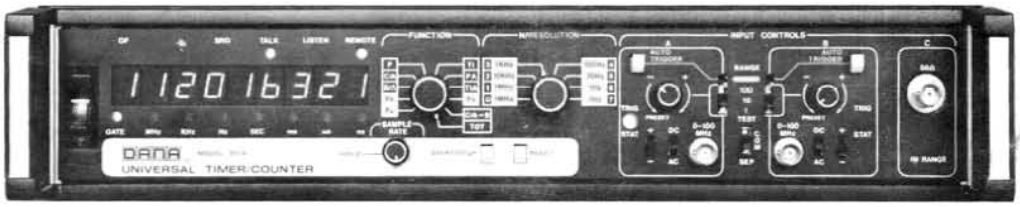
MAINTENANCE MANUAL

9500

UNIVERSAL TIMER/COUNTER



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9500
UNIVERSAL TIMER/COUNTER

MAINTENANCE MANUAL

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Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltages hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC Mains through an autotransformer (such as a Variac or equivalent) ensure that the instrument common connector is connected to the ground (earth) connection of the power mains.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adapter.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument.

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation section.
2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.
3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

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SECTION 1 THEORY OF OPERATION

1.1 GENERAL.

This section describes the theory of operation of the Series 9500 Timer/Counters. The Series 9500 Timer/Counters include the Model 9510 and 9514. The descriptions in the following paragraphs generally refer to both instruments. Specific differences are noted in appropriate paragraphs for clarity.

1.1.1 The theory of operation in this section is first analyzed in terms of the simplified block diagram shown in figure 1.1; second, the various operating modes are described; and third, individual circuits are described.

1.1.2 The drawings and diagrams included in this section are for aiding in the descriptions and are provided as a supplement to the complete schematics in Section 3.

1.2 OVERALL THEORY OF OPERATION

1.2.1 The Series 9500 Timer/Counters are shown in block diagram form in figure 1.1. Input signals to be measured can be applied to the signal conditioners through front panel jacks for channels A, B, and the optional RF channel C or through the rear panel to the same channels. Front panel controls or the microprocessor (Model 9514 only) activate the control circuits to make the selected measurement at the selected resolution. Depending on the function selected, either the input signal or the time base signal is routed to the accumulator. Input signals are processed in the signal conditioners to limit the amplitude and convert the signal to a digital signal that is compatible with the counter logic.

1.2.2 Input channels A and B are identical through the signal conditioning circuits. The high frequency channel C circuit is an optional plug-in board which includes a signal conditioner for the 50 to 500 MHz range. The signal conditioning circuits contain the AC/DC coupling circuits, the attenuator, the signal conditioning amplifiers and schmitt trigger circuits to condition and convert the measurement signal to a digital signal. The conditioned measurement signals are routed to the input selection circuit which in turn routes them to the gate control or to the main gate depending on the function and mode selected. As shown on the diagram, the selected measurement signal may be used as the count signal while the gate control signals control the flow of the count to the accumulator. For example, when measuring frequency in the FA mode the selected measurement signals are applied to the main gate and the start/stop signals from the time base generator through the input selection logic produce the gate which gates the count signals to the accumulator. In this situation the count signal is the FA selected measurement and the gate signal is the time base gate.

1.2.3 The converse is true in some functions such as time interval measurement. In time interval mode the conditioned measurement signals are used to produce the START/STOP signal for the gate control and thus the gate control produces the gate signal to control the main gate. The count signal is a clock signal derived from the master oscillator clock signal.

1.2.4 The conditioned measurement signals are also routed from the signal conditioning circuits to the marker generator. The marker generator circuit produces an external marker useful for observing the measurement time on an oscilloscope. The marker signal starts when channel A triggers and terminates when channel B triggers. The marker pulse represents the precise measurement of the time between channel A and channel B triggering. The trigger levels can be adjusted accurately with the use of an oscilloscope and the external marker. The oscilloscope trace displays the point where the time measurement starts and terminates.

1.2.5 The counter uses an internal master oscillator which produces a 10 megahertz clock signal for a measurement reference. There are three choices of master oscillator for the instrument. The output of the master oscillator can be routed to the reference connector through appropriate switching on the rear panel of the instrument.

1.2.6 In some applications it is desirable to use an outside reference frequency for the master reference of the 9500 timer-counter. In this application the external reference frequency is applied to the REF connector on the rear panel and the instrument then uses the external reference as a substitute for the internal master oscillator. An external signal should not be connected to the connector when the instrument is operating on the internal reference oscillator.

1.2.7 Some users of the instrument may wish to connect a 1 MHz or a 5 MHz external reference signal to the instrument and for this purpose an optional reference multiplier is available. The reference multiplier will multiply the 1 MHz or 5 MHz signal and produce the 10 MHz reference frequency for use as the timebase clock.

1.2.8 The function, range and mode of the instrument is controlled through front panel controls which apply control signals to the control logic. The control logic applies the appropriate control codes to the input selection logic and gate control circuits causing the instrument to perform the desired function.

1.2.9 During the measurement cycle the gated count is applied to the accumulator for the measurement gate period. After the main gate is closed the contents of the accumulator are displayed on the front panel display.

1.2.10 General Purpose Interface Bus

1.2.10.1 The Model 9514 includes a general purpose interface bus (GPIB). This is shown on the block diagram below the dotted line. When the GPIB is used, control signals from the interface bus applied to the program input section of the GPIB circuits generate control signals as substitutes for the control signals from the front panel controls. Thus, the system, or external controller, is enabled to operate the instrument remotely. Measurement information from the accumulator is routed to the GPIB circuits for transmission over the interface bus to the controller or system.

1.2.11 Measurement Gate Control

1.2.11.1 The measurement (main) gate controls the length of time that the input signal, time base signal, or reference frequency is counted in the accumulator. The opening and closing of the measurement (main) gate is controlled by the gate control circuit. The gate control circuit can be armed; that is prepared to start, internally at a regular rate, or externally with a control signal applied to the GATE CONTROL connector on the rear panel. When the measurement gate is opened, the selected signal is counted in the accumulator until the gate is closed. The BCD equivalent of the registered count is strobed in multiplexed form into each digit on the front panel and displayed for the amount of time set by the SAMPLE RATE/HOLD control.

1.2.11.2 To provide a wide variety of measurement application capabilities the 9500 Series Timer/Counters are equipped with special circuits which allow control of the measurement gate start and stop time by external means. In normal operation the measurement gate control is a function of the measurement mode and input channel selection. When the channel A input is used the measurement gate will not open until the measurement signal applied to the channel A input is of sufficient magnitude to trigger the instrument. Channel B on the other hand is designed for continuous arming and the measurement gate is under control of the sample rate control on the front panel. Control of the measurement gate may be accomplished by an external control signal applied to a connector on the rear panel of the instrument. Selection of the measurement gate control mode is accomplished by setting a switch on the rear panel of the instrument. When the Model 9514 is operated in the system mode, selection of the measurement gate control may be done by system commands via the general purpose interface bus. The description of the measurement gate control operation in the various modes is presented in the following paragraphs.

1.2.11.3 SELECTIVE GATE CONTROL.

1.2.11.3.1 It is often necessary to measure the period of a train of pulses or electrical events as opposed to the period of a single event. This is easily accomplished with the Selective Gate Control. By applying a positive going TTL pulse to the gate control input, the counter's measurement gate can be controlled so that the measurement encompasses the desired period. The rising edge of the TTL pulse arms the counter to trigger at the first correct trigger point to begin the measurement. The high level of the TTL pulse inhibits the measurement gate from closing. Thus, the measurement gate is held open until the external gate control signal goes low. The falling edge of the external gate control signal then enables the counter to terminate the measurement when the next correct trigger point occurs.

1.2.11.4 SYNCHRONOUS WINDOW CONTROL.

1.2.11.4.1 The Synchronous Window feature is used to isolate a pulse or a period of time during which the 9500 is to make a timing measurement. By moving the time position of the synchronous window control pulse and by varying the width of

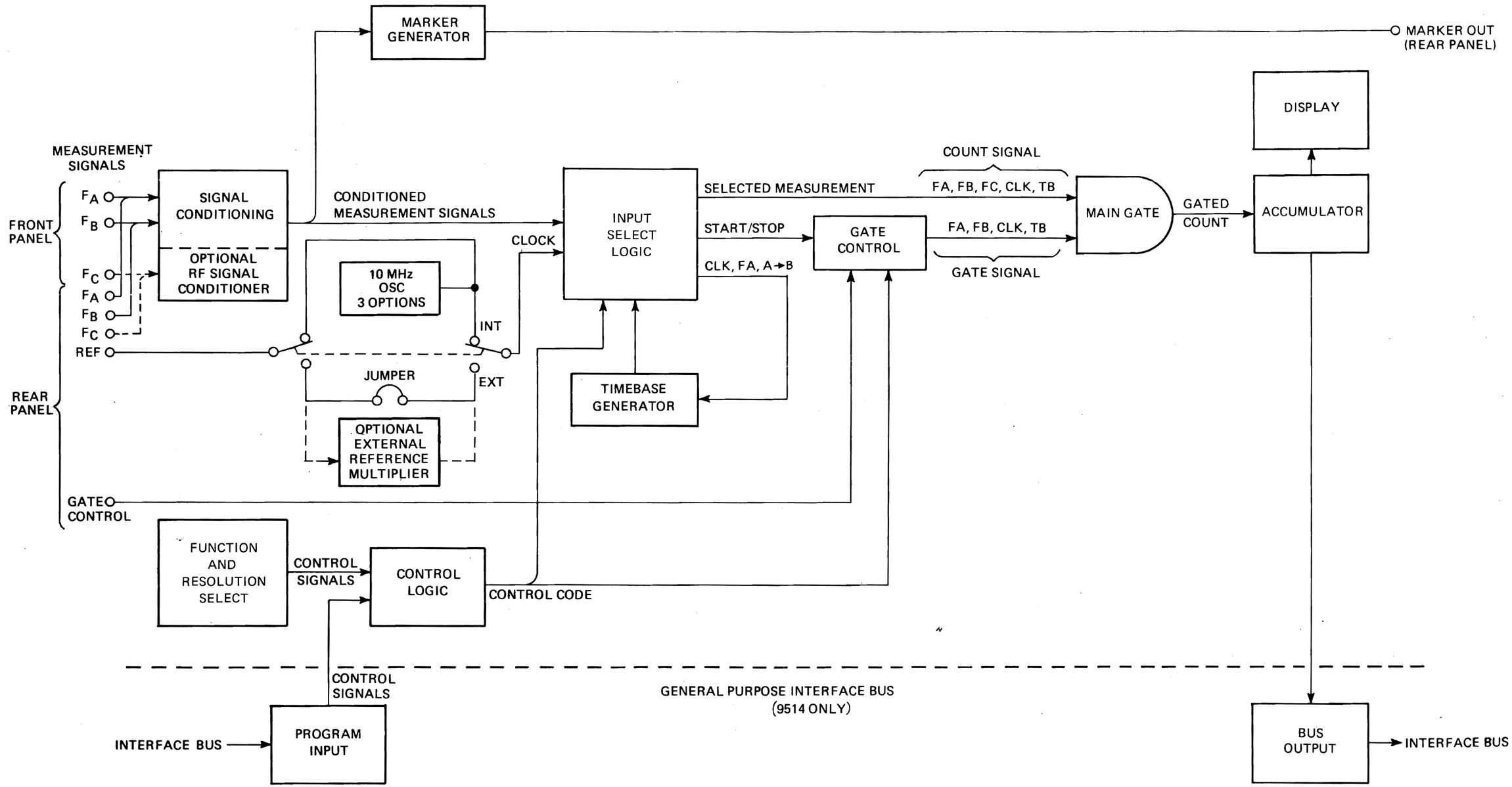

Figure 1.1 - Series 9500 Timer/Counter Functional Block Diagram

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the pulse a selective measurement window is created which defines the area of time during which the 9500 will make its measurement.

1.2.11.4.2 In the time interval average measurement mode an externally applied pulse controls the arming of channels A and B. The rising edge of the positive going TTL pulse enables both channels to trigger at the next set of correct trigger points. The falling edge disables both channels. Consequently the measurement window is created during which time the 9500 can make a measurement.

1.2.11.5 GATE DELAY.

1.2.11.5.1 This mode of measurement is very similar to the selective gate mode except that the counter does not arm at the rising edge of the control waveform. The counter is prevented from finishing a measurement whenever the control waveform is at a high level. A typical application of this mode is the measurement of time between RF bursts (less than 100 megahertz) and a control signal is not available (i.e., the selective gate mode cannot be used). In such a case the time interval mode is selected, the gate output signal from the counter is used to trigger a pulse generator and the pulse generator is adjusted to provide the control waveform whose duration is longer than the RF burst. Thus, the incoming RF measurement burst signal will trigger the counter and the control waveform from the pulse generator will prevent the counters measurement gate from closing until the arrival of the next RF burst.

1.2.11.6 EXTERNAL ARM.

1.2.11.6.1 The instrument may be externally armed by use of a control signal applied to the gate control connector on the rear panel when operating on the standard interface bus. This allows the controller or system to control the trigger arming remotely while in the system mode of operation. This feature is available on the Model 9514 instrument only and is not available for bench operation.

1.3 MEASUREMENT MODES.

1.3.1 The function selected modifies the routing of both the input signal or signals and the reference signal. These differences in instrument operation are described in the following paragraphs. For simplicity in the accompanying figures, the accumulator counters are shown driving the display.

1.3.2 Test.

1.3.2.1 The TEST mode of operation (figure 1.2) enables the operator to check for proper operation of the counter.

1.3.2.2 In the TEST mode the reference signal is used in place of the outputs from channel A and channel B. The reference signal then is counted in the accumulator and the results displayed on the front panel.

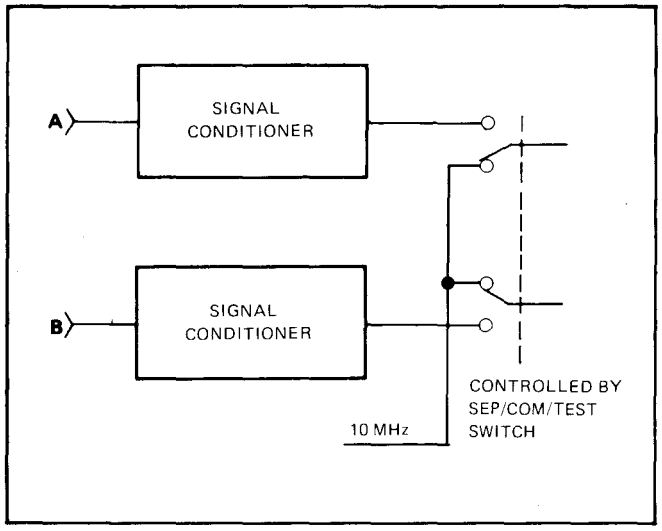


Figure 1.2 - Test

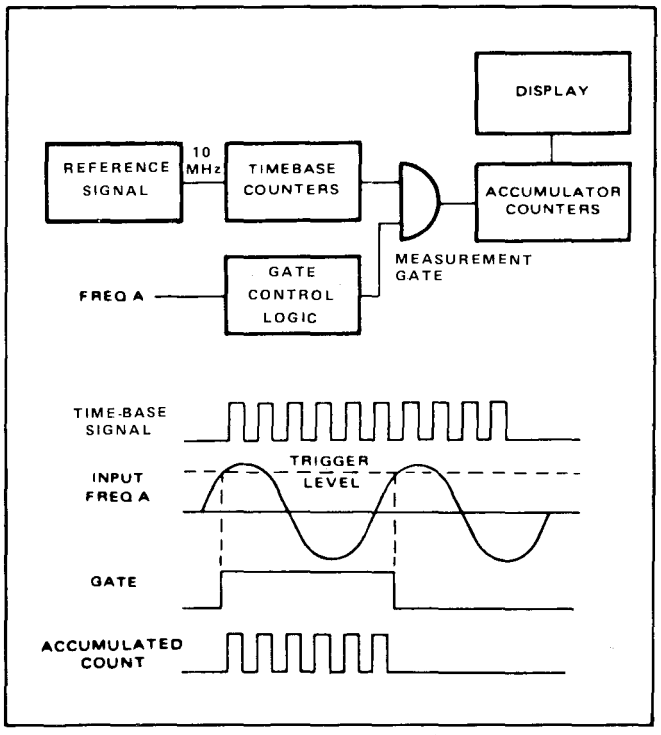


Figure 1.3 - Period

1.3.3 Period.

1.3.3.1 Period is the inverse of frequency. Therefore, channel A signal is applied to the gate control logic and the reference signal is connected to the time base counters (figure 1.3).

1.3.3.2 Clock pulses are derived by dividing down the 10 MHz reference. The specific decade division is determined by the setting of the N/RESOLUTION switch. The output of the time base counters is presented to the input of the accumulator counters. Trigger pulses resulting from two consecutive signals from input A are applied to the control logic. The first trigger pulse opens the main gate; the next pulse closes it. During gate-open time, the counter counts the applied clock pulses. The count is displayed on the readout directly in microseconds, milliseconds, or seconds, according to the N/RESOLUTION switch setting.

NOTE

Low frequencies may be determined more accurately by measuring period rather than frequency directly. This is because the longer period of a low frequency allows more counts to accumulate in a period measurement. Therefore, resolution and accuracy are both improved.

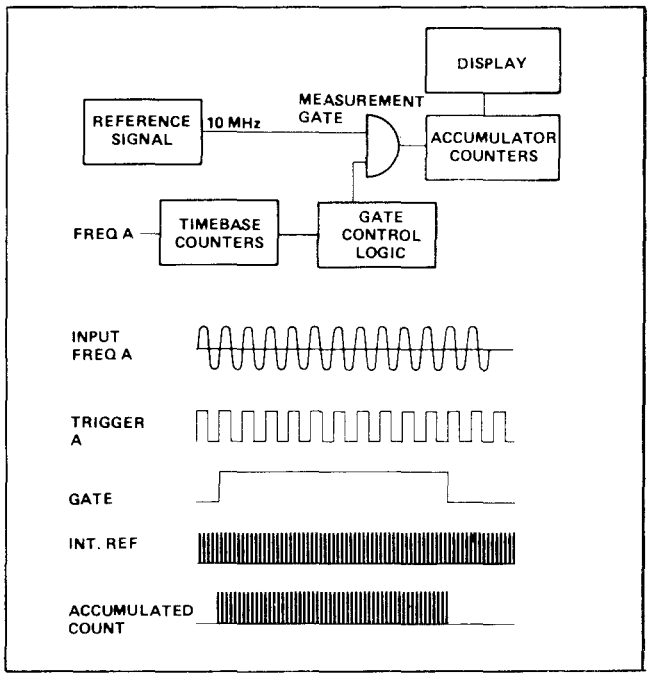


Figure 1.4 - Period Average

1.3.4 Period Average.

1.3.4.1 Period Average mode is used to obtain increased resolution and accuracy over period measurements. The more periods over which a signal is averaged, the greater the accuracy of the measurement.

1.3.4.2 In this mode of operation (figure 1.4), the reference signal is routed directly to the measurement gate and the unknown signal is routed through the time base to the control logic which, in turn, controls the measurement gate. The pulses occurring during measurement gate-open are counted, stored, and an accurate readout measurement is displayed. The gate-open period is determined by the time base selected.

1.3.5 Frequency A.

1.3.5.1 During direct frequency measurements, the counter compares the unknown frequency against the known reference frequency (figure 1.5).

1.3.5.2 Channel A input signal is routed to the measurement gate of the counter. The internal reference signal supplies a 10 MHz signal through the time base and through the gate control logic to control the measurement gate.

1.3.5.3 The number of input pulses accumulated during the gate-open interval is a measurement of the input frequency. The count obtained is displayed on the readout. This display may be retained until such time as a new sample is ready to be displayed.

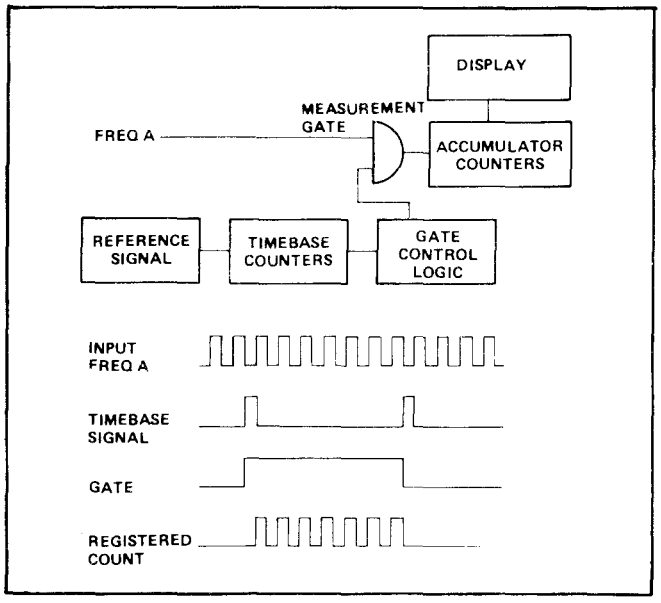


Figure 1.5 - Frequency A

1.3.6 Frequency C

1.3.6.1 In the Frequency C mode, the signal of unknown frequency is applied to the accumulator through the RF option board. The RF option includes an amplifier, detector circuit, and a divide-by-ten counter (figure 1.6).

1.3.6.2 The detector circuit provides an indication of the minimum required signal for reliable operation. The divide-by-ten counter is necessary to reduce the unknown frequency to a frequency which the main counter circuitry can count.

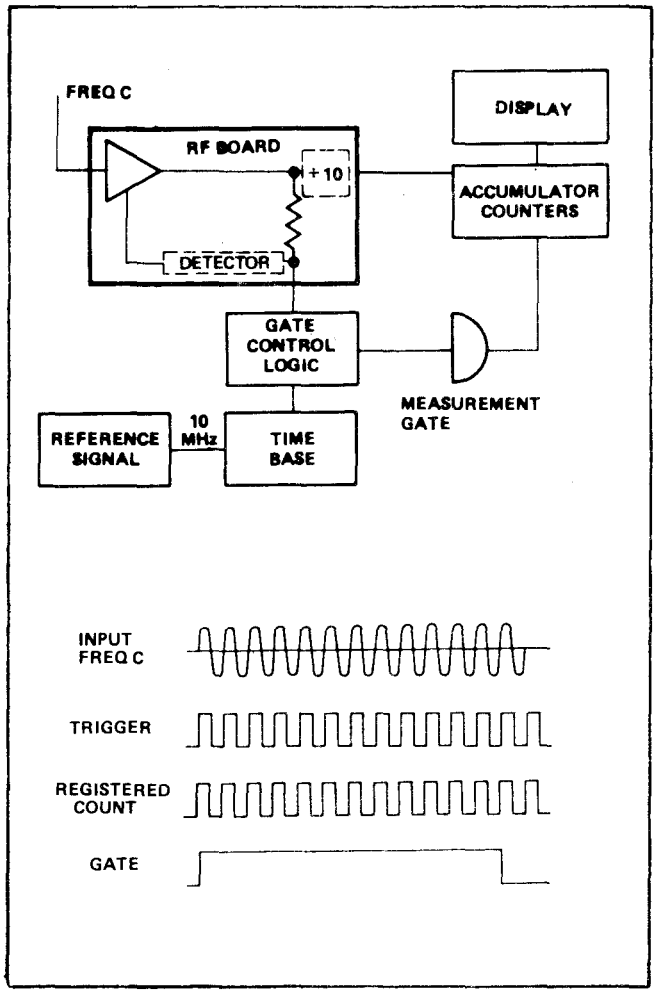


Figure 1.6 - Frequency C

1.3.7 Totalize.

1.3.7.1 In Totalize mode, the main gate is controlled by the manual START/STOP switch on the front panel or external START/STOP commands (figure 1.7).

1.3.7.2 With the first Start/Stop command, the control logic opens the measurement gate allowing the input pulses to be totalized by the counter. The counter readout then represents the input pulses received during the interval between start and stop. External start/stop commands may be applied via the GPIB (9514 Model only).

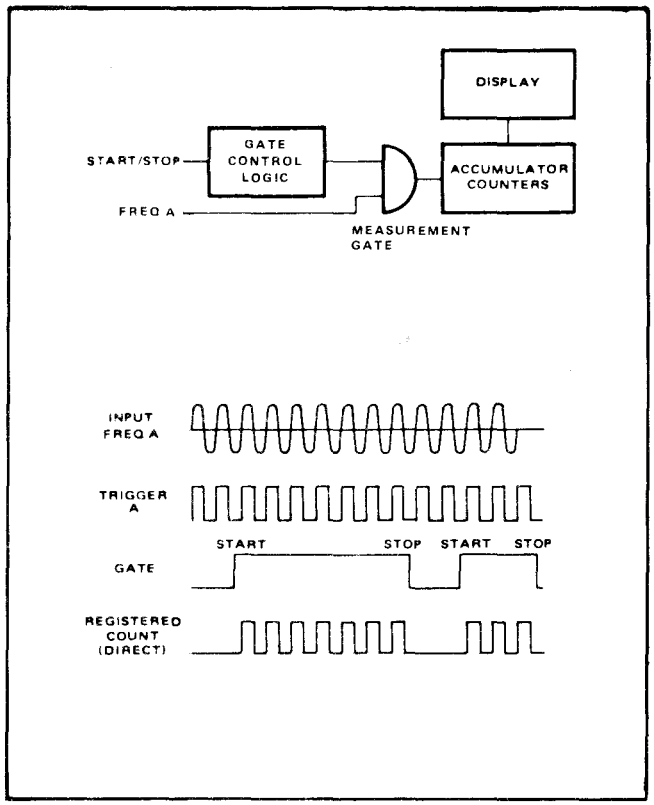


Figure 1.7 - Totalize

1.3.8 Time Interval.

1.3.8.1 The Time Interval mode of operation allows measurement of the time between two electrical events to a maximum resolution of 100 nanoseconds (figure 1.8). The first event (start) is connected to channel A and opens the gate. The second event (stop) is connected to channel B and closes the gate. These signals control the main gate through the control logic. Slope and trigger level programming allow variable trigger levels on the + or – slope of the input waveforms. Pulses from the 10 MHz reference circuit are routed to the time base and to the measurement gate. The pulses occurring during the gate are counted and displayed.

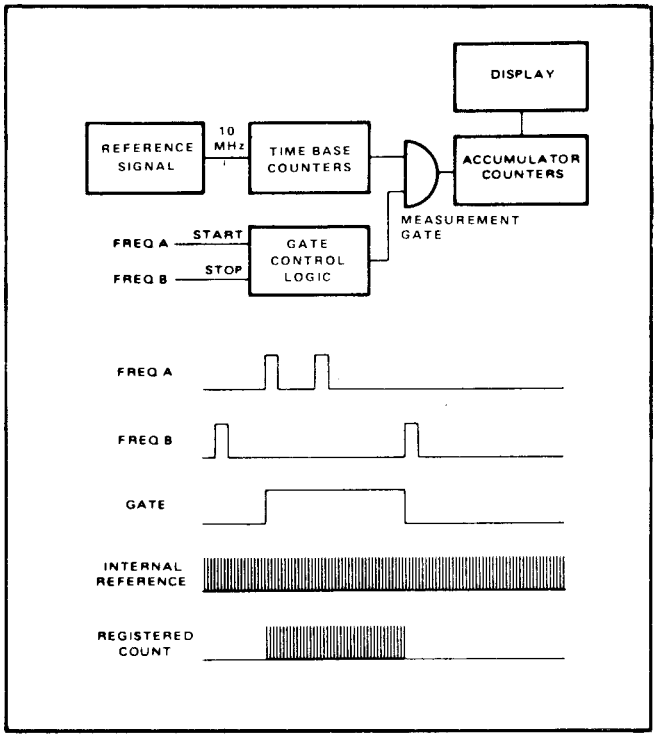


Figure 1.8 - Time Interval

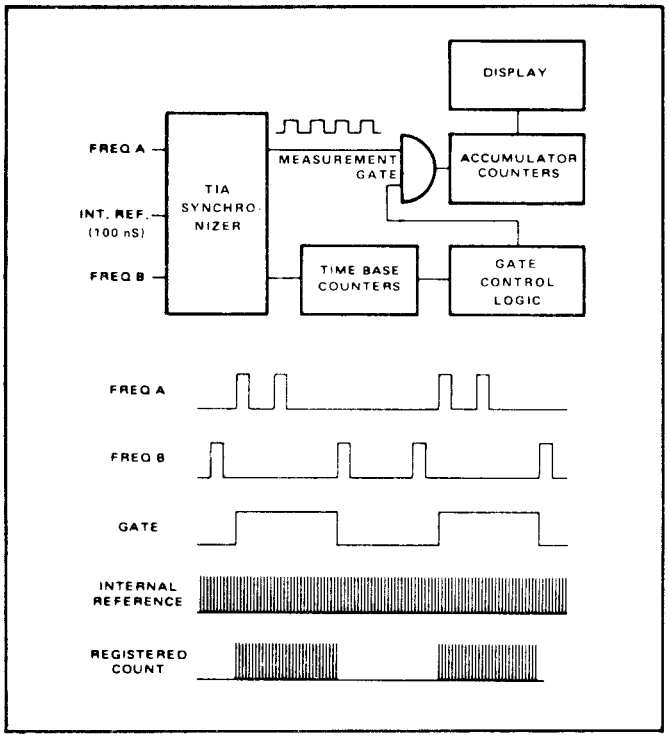


Figure 1.9 - Time Interval Average

1.3.9 Time Interval Average.

1.3.9.1 Similar to the Time Interval mode of operation, the Time Interval Average mode measures the count accumulated during a multiple of intervals (figure 1.9). It then averages the count by shifting the decimal point and displaying the result. This mode of operation makes it possible to achieve greater resolution and accuracy when measuring time intervals. The A trigger point can follow the B trigger point as close as 200 nanoseconds.

NOTE

In T.I. Average mode, the input signals must be repetitive and asynchronous with the counter's time-base.

1.3.10 B/A (Ratio).

1.3.10.1 This mode is identical in function to the frequency measurement modes, but substitutes an external signal for the reference signal (figure 1.10).

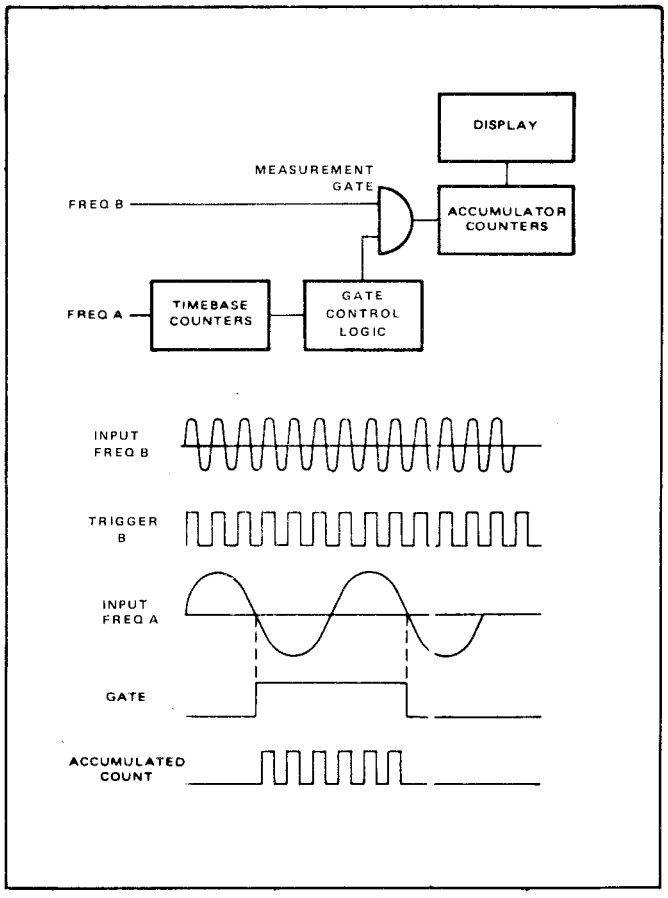


Figure 1.10 - B/A Ratio

1.3.10.2 The higher of the two frequencies which are to be measured is connected to input B; the lower frequency to input A. Input A is applied to the time base counters. The higher the time base selected, the greater the resolution and the longer the measurement time. Two successive positive going edges derived from the time base counters resulting from the input A, open and close the main gate. During the gate-open interval, the counter counts the trigger pulses derived from input A and the ratio fb/fa is then displayed on the readout.

1.4 DETAILED THEORY OF OPERATION.

1.4.1 Individual circuit theory of operation is described in this section. The diagrams used in this section are simplified schematics or functional block diagrams. For complete schematic diagrams, refer to Section 6.

1.4.2 Table 1.1 contains a list of signals used in the Series 9500 Timer/Counters. Signals used together are grouped together. The function of each signal or group of signals is described and significant sources or destinations are noted.

1.4.3 Table 1.2 contains a list of signal requirements for each measurement function. Corresponding to each measurement function in the first column is the signal to open and close the measurement gate, the signal counted in the accumulator, and the time base signal. In the synchronizer column, the state of the GOSC or $\overline{A \rightarrow B}$ signal is listed. The reclocked time base column lists whether the reclocked time base is required. In the next column, the source of the least significant digit BCD data is listed and in the last column the timing logic mode is shown.

Table 1.1 - Signal Functions

Signal	Function
$\overline{A \rightarrow B}$	TIA Synchronizer signal. Its width represents the time interval being averaged.
AB1, AB2, AB4	Annunciator bits.
ARM	Output signal of the arming flip-flop. Sets the D-input of the start flip-flop to open the measurement gate.
ATE	Automatic trigger enable signal.
B0, B1, B2	Select the input control signals to start and stop the measurement gate.
B2	Time base enable signal in frequency function.
B5	Accumulator input enable signal in frequency A and totalize functions.
B6	Time base enable signal in period and time interval functions.
B7	Accumulator input enable signal in period average function.
B8	Accumulator input enable signal in frequency B and ratio functions.
B10	Presets the TIA Synchronizer flip-flops.
B11	Enables the TIA Synchronizer for Channel C timebase control.
CARM	Arming signal from RF option board.
$\overline{\text{CLEAR}}$, CLEAR	Clears the accumulator; sets time base decade counters to all nines.
$\overline{\text{CRES}}$	Input channel C reset signal.

Table 1.1 - Signal Functions continued

Signal	Function
DPB1, DPB2, DPB3	Octal select code for decimal point strobes.
$\overline{\text{DRDY}}$	Data ready signal indicates that the reading is completed and the output is stable.
$\overline{\text{DRES}}$	Data reset signal to generate $\overline{\text{LOAD}}$.
DRTB	Double reclocked time base signal.
EA	External arm signal applied to rear panel gate control.
$\overline{\text{EAEL}}$	External arm enable local signal.
$\overline{\text{EAER}}$	External arm enable remote signal.
fa	Input signal applied to the A-input on the front panel to be measured.
fa (TTL), fb (TTL)	Channels A and B signal conditioner signals translated to TTL logic levels.
fr	10 MHz reference clock signal
FA, FB, FC, FD	Function switch output signals to generate control signals B0 through B17.
$\overline{\text{GATE}}$	Low when measurement gate is open.
$\overline{\text{GDL}}$	Gate delay local signal.
$\overline{\text{GDR}}$	Gate delay remote enable signal from GPIB
GDY	Gate delay signal to keep measurement gate open.
GOSC	Gated oscillator signal. Used in time interval average measurements.
$\overline{\text{LIST}}$	GPIB signal to front panel LED.
$\overline{\text{LOAD}}$	Transfers the contents of the accumulator to the display.
$\overline{\text{LT}}$	Lamp test signal generated by front panel RESET switch to illuminate all displays and decimal points.
$\overline{\text{MARKER OUT}}$	Rear panel output coinciding with Channel A and B triggers.
$\overline{\text{MLCL}}$	Main logic clear signal from the GPIB.
OF	Overflow in the display.
$\overline{\text{POR}}$	Power on reset.

Table 1.1 - Signal Functions continued

Signal	Function
RA, RB, RC	Time base frequency select signals from the resolution switch.
RBI	Ripple blanking input.
RBO	Ripple blanking output.
$\overline{\text{RES}}$	Reset from RESET switch.
$\overline{\text{RMT}}$	Remote signal to disable local operation from GPIB.
$\overline{\text{RTL}}$	Return to local control. Requests that the microprocessor return measurement control to front panel switch settings.
$\overline{\text{S/SR}}$	Start/stop remote signal.
STA, STB, STC, STD	LS7031 counter multiplexed BCD output.
SCAN	External strobe frequency from the GPIB to the accumulator counter.
SCRS	Scan reset signal to the LS7031 counter and data ready flip-flop.
$\overline{\text{SLV}}$	Indicates whether the measurement signal is above or below the trigger level.
SPR	Sample rate signal from front panel potentiometer to display timeout circuit
SRBI	Strobed ripple blanking input from the accumulator to the display.
$\overline{\text{SRQ}}$	Service request signal from GPIB to front panel LED.
$\overline{\text{SXL}}$	Indicates that the measurement signal has crossed the trigger level.
$\overline{\text{SWL}}$	Synchronous window local select signal.
$\overline{\text{SWR}}$	Synchronous window remote enable signal from GPIB.
S1 – S8	Accumulator counter stroke lines to display.
$\overline{\text{TALK}}$	GPIB signal to front panel LED.
TB	Time base output signal. In the period or time interval mode available selections are 1, 10, and 100 Hz; 1, 10, and 100 kHz; and 1 and 10 MHz.
$\overline{\text{UPDATE}}$	Generated by the closing of the measurement gate. Loads accumulator contents into the display. Starts display timeout circuit.
$\overline{\text{UPDR}}$	Remote update signal from GPIB.

Table 1.2 - Signal Requirements For Measurement Functions

Function	Gate	Accumulator Signal	Time Base	Synchronizer	Reclocked Time Base	Least Significant Digit	Timing Logic
F_A	DRTB ⌐ DRTB ⌙	fa	1 MHz	fa arm/$\overline{A \rightarrow B}$ low/GOSC	Yes	Main	Normal
F_C	DRTB ⌐ DRTB ⌙ RF enabled	fc	1 MHz	fc arm/$\overline{A \rightarrow B}$ low/GOSC	Yes	RF	Normal
R_B	TB ⌐ TB ⌙	fb	fa	high/$\overline{A \rightarrow B}$ low/GOSC	Don't care	Main	Normal
R_C	TB ⌐ TB ⌙ RF enabled	fc	fa	high/$\overline{A \rightarrow B}$ low/GOSC	Don't care	RF	Normal
P	fa ⌐ fa ⌙	TB	10 MHz	high/$\overline{A \rightarrow B}$ low/GOSC	Inhibit	Main	Normal
TI	fa ⌐ fb ⌙	TB	10 MHz	high/$\overline{A \rightarrow B}$ low/GOSC	Inhibit	Main	Normal
PA	TB ⌐ TB ⌙	10 MHz	fa	high/$\overline{A \rightarrow B}$ low/GOSC	Don't care	Main	Normal
TIA	TB ⌐ TB ⌙	GOSC	A→B intervals	$\overline{A \rightarrow B}$ int./$\overline{A \rightarrow B}$ 10 MHz·A→B/GOSC	Don't care	Main	Normal
C/A→B	fa ⌐ fb ⌙ RF enabled	fc	10 MHz	don't care/$\overline{A \rightarrow B}$ low/GOSC	Inhibit	RF	Normal
TO	S/S ⌐ S/S ⌙	fa	10 MHz	don't care/$\overline{A \rightarrow B}$ low/GOSC	Inhibit	Main	Manual CLEAR; UPDATE to display continuous

1.4.4 Input Attenuator and Buffer

1.4.4.1 The input attenuator and buffer circuits provide control of measurement signal range selection, channel A and B input configuration, trigger level control, slope selection and a self test feature of the counter. In addition, these circuits provide high impedance input to prevent loading of the circuit under test and a signal level of sufficient current drive for application to the signal conditioning circuits.

1.4.4.2 A simplified diagram of the input attenuator and buffer is presented in figure 1.11. A review of the simplified diagram and of the schematic in the drawing section of this manual will show that the channel A and B input attenuator and buffer circuits are identical except for the input configuration switch circuitry. The input configuration switch is labeled separate (SEP), common (COM) and test. When the switch is in the SEP position as shown on the simplified diagram, the channel B input connector is connected through the input configuration switch to the channel B coupling switch and capacitor. The channel A input connector is always connected directly to the channel A coupling switch and AC coupling capacitor.

1.4.4.3 When the input configuration switch is set to the common position the channel B input connector is disconnected and the channel A input connector is connected to the channel B coupling switch. The signal applied to the channel A input connector is re-routed both to channel A and to channel B attenuator and buffer circuits.

1.4.4.4 When the configuration switch is set to the test position the input attenuator and buffer circuits are not in use. Note that the second set of contacts on the configuration switch when the switch is set to the test position connect the $\overline{\text{TEST}}$ to ground. This is a signal line which is routed to the signal conditioning circuits and when grounded this signal line causes the signal conditioning circuits to gate in a 10 megacycle reference signal for use as a input test signal.

1.4.4.5 The channel A and channel B input attenuator and buffer circuits are identical. And thus the following discussion of the channel A circuits applied also to the channel B circuits. The measurement signal is routed through the coupling switch or AC coupling capacitor. When the coupling switch is set to the DC position it is closed and the capacitor is out of the circuit. When the switch is open the measurement signal is routed through the AC coupling capacitor to the high frequency current limiting resistor. This resistor is a relatively low value (43 ohms) and is in the circuit to prevent the flow of high current at high frequencies during overload conditions. The high frequency current limiting resistor is located in the input buffers and will be discussed in paragraphs to follow.

1.4.4.6 Attenuation of the measurement input signal is accomplished by the range switch and associated attenuation resistors and compensating capacitors. There are 3 input attenuation ranges; X 1, X 10 and X 100. The measurement signal input ranges are 0 to ± 3 volts, 0 to ± 30 volts and 0 to ± 300 volts respectively.

1.4.4.7 The measurement signal output of the attenuator switch is applied to the high impedance buffer amplifier Q3 (in the case of channel A), a unity gain FET amplifier. This amplifier provides the high impedance input necessary to prevent the counter from loading the circuit under measurement. The output of the high impedance buffer amplifier is applied to the low impedance driver Q1 (in the case channel A). The low impedance driver amplifier provides the signal drive output capability necessary to provide the signal conditioners with a measurement signal of sufficient amplitude to operate the counter circuits.

1.4.4.8 The signal conditioning circuits are provided with a trigger level signal by the trigger circuits which are a part of the input attenuator and buffer circuits. In the Model 9510 trigger level control is accomplished manually through the use of front panel potentiometers and the associated preset switch. The preset trigger level voltage is derived by the trigger level A potentiometer. This potentiometer is connected across a trigger reference voltage and rotating the potentiometer control picks off a varying voltage level to set the triggering point of the signal conditioning circuits as a counter. The triggering level is adjustable from -3 volts to $+3$ volts depending on the position of the trigger level control.

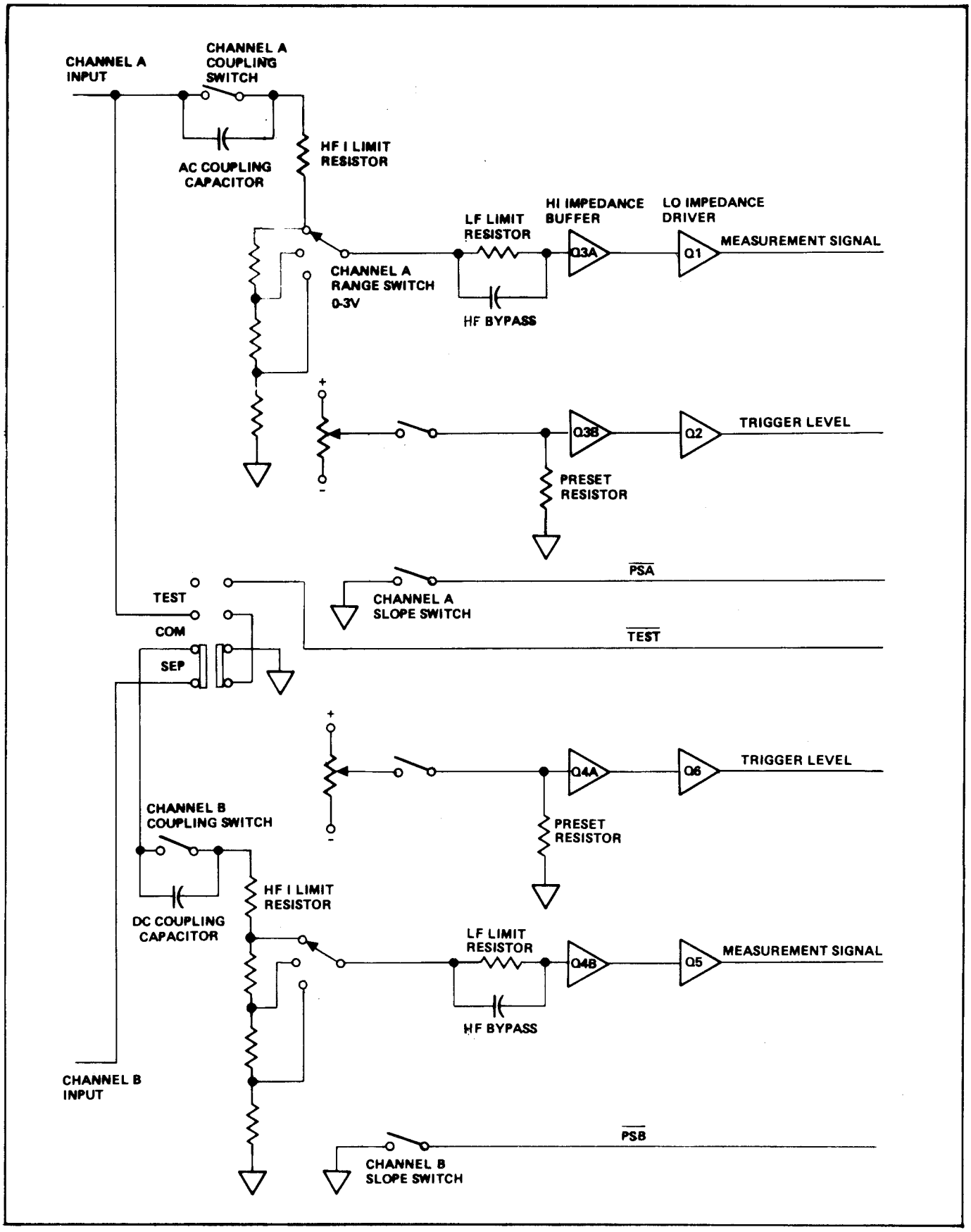


Figure 1.11 - Input Attenuator and Buffer Simplified Diagram

1.4.4.9 A trigger level may be preset so that the counter triggers as the signal crosses 0 volts by rotating the trigger level control to the full counterclockwise position. In the fully counterclockwise position the preset switch mechanically coupled to the trigger level control opens and thus the trigger level voltage from the trigger level control is disconnected from the input of the high impedance buffer. The trigger voltage is determined by a fixed resistor which is connected from the high impedance buffer gate to ground.

1.4.4.10 The high impedance buffer and low impedance driver for the trigger level circuits are identifical to those for the measurement signal buffers. The trigger level signal and measurement signals share a common dual FET and thus are subject to the same temperature conditions during operation. These circuits are configured in this manner so that any change of measurement level in the buffer circuits will be followed by a change in the trigger level circuits. Thus the measurement level and trigger level buffers will track as the ambient temperature changes.

1.4.4.11 SCHMITT TRIGGER

1.4.4.11.1 The Schmitt trigger circuit converts the input signal into a square-wave signal, by switching action, triggered at a predetermined point in each positive and negative swing of the input signal. See figure 1.12. The level at which the circuit triggers is dependent on the reference input supplied by the trigger level and is not equal for both the positive and negative going portion of the input waveform; that is, the circuit displays a fixed amount of hysteresis. For measurements of frequency and period, hysteresis is an advantage in that it reduces false triggering at low amplitude levels; for measurement of time interval and time interval average, however, a means of compensating for the hysteresis is needed. Hysteresis compensation is provided to ensure precise switching at the same point on both positive going and negative going signals. The hysteresis compensation circuit shifts the dead band so that the Schmitt trigger fires on the same point rising as falling.

1.4.4.11.2 The hysteresis compensation circuit consists of a differential output current source, activated when TI or TIA is selected. The circuit draws a fixed amount of calibrated current from the inverting or non-inverting input circuitry of the Schmitt trigger according to whether + slope is selected or not. The result is to cause the trigger circuit to trigger at the same voltage level on the positive and negative slope of the input signal.

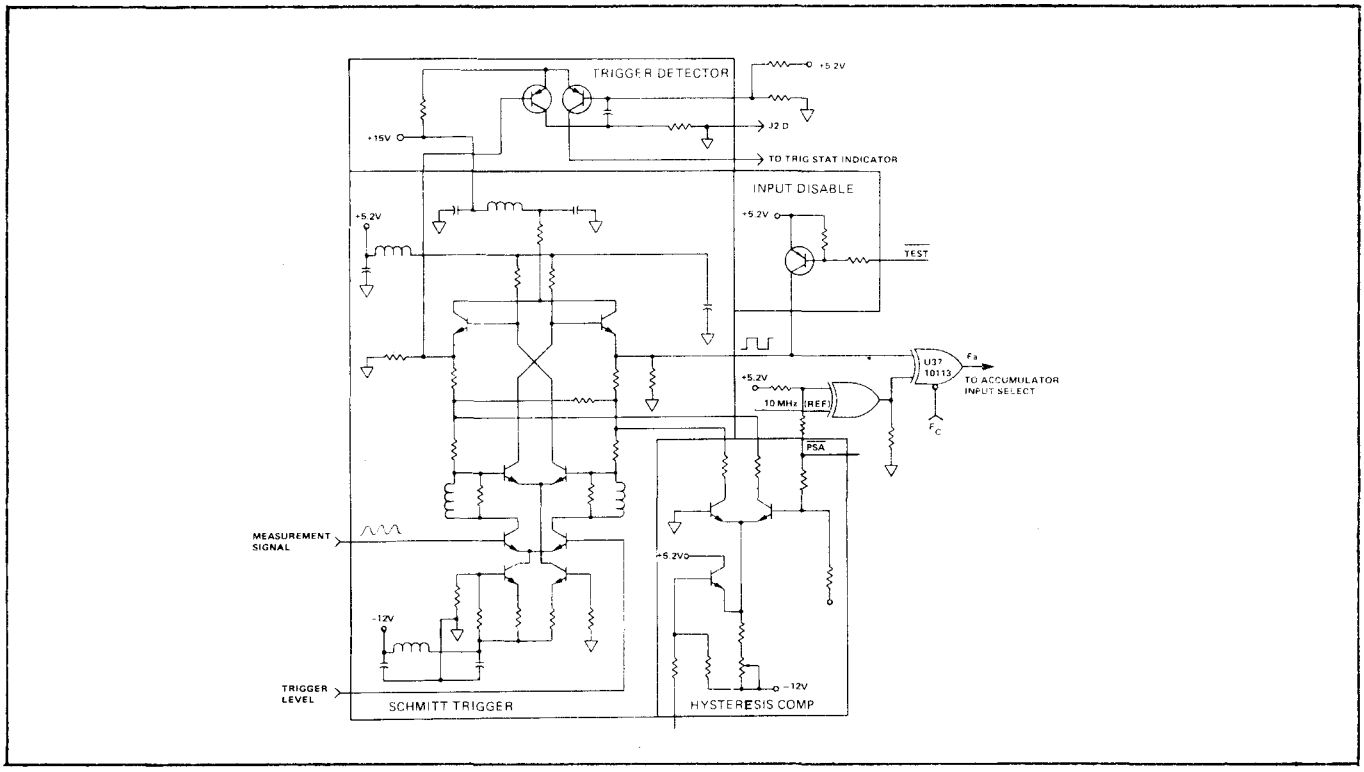


Figure 1.12 - Simplified Schmitt Trigger Schematic Diagram

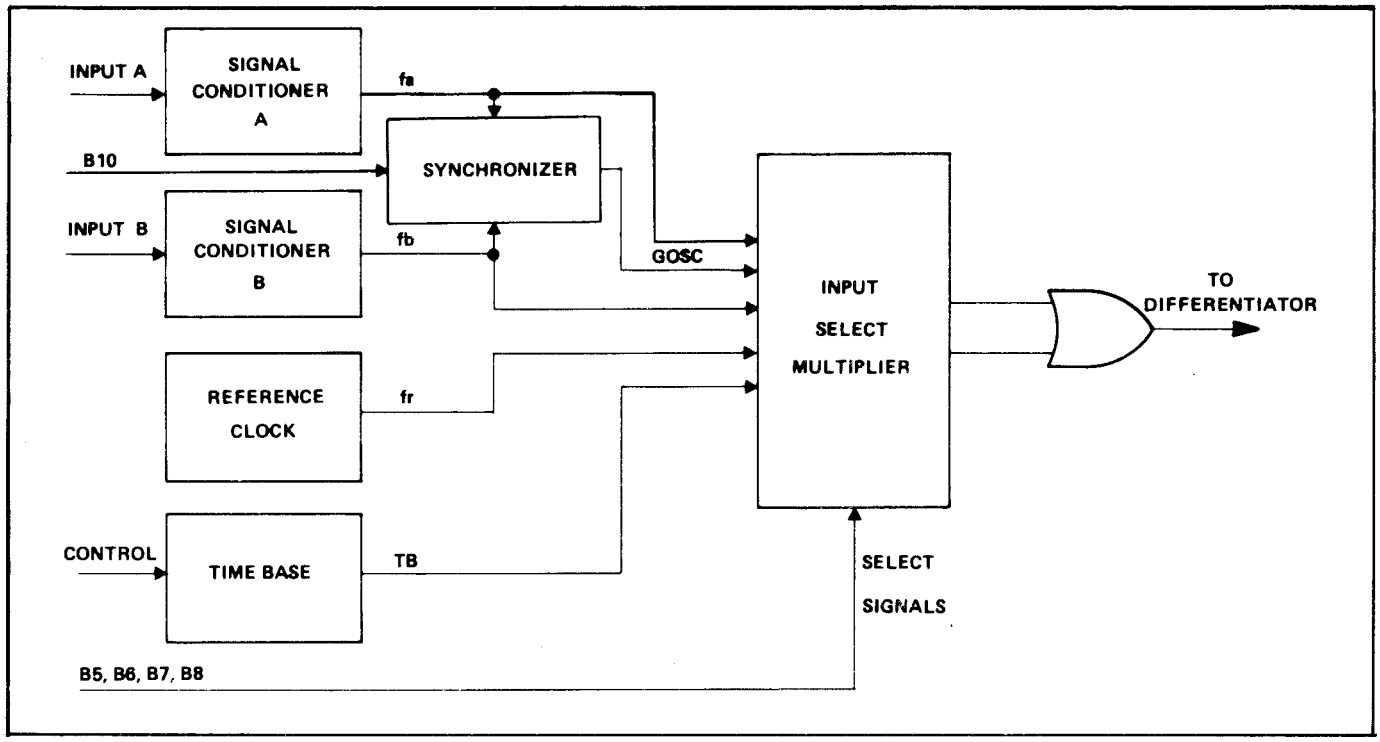


Figure 1.13 - Input Select Logic

1.4.4.12 TRIGGER DETECTOR

1.4.4.12.1 The trigger detector is a timing circuit that indicates an output out of the Schmitt trigger. The indication is that an input signal has overcome the trigger level and fired the Schmitt trigger. The trigger detector slows the rate of the detected signal and sends the slower rate to blink the front panel TRIG STAT indicator. When the trigger level is set above the signal the TRIG STAT indicator stays on continuously, and when the trigger level is set below the signal the indicator remains off.

1.4.5 Accumulator Input Selection

1.4.5.1 The accumulator input select logic selects the signal determined by the function set on the front panel FUNCTION switch or programmed by a remote controller via the interface bus. A functional block diagram of the input select logic is shown in figure 4.13. The input logic select circuit is a five-to-one multiplexer. One of fa, fb, fr, GOSC, or TB is selected. The counter input select logic is comprised of both TTL and ECL logic. The ECL level signals fa and fb from the Schmitt trigger are applied directly to the input select logic. The TTL control signals are translated from TTL logic levels to ECL logic levels in a resistive network prior to input selection. The control signals necessary for signal selection are listed in table 1.3. This input selection logic selects only those signals whose destination is the accumulator.

Table 1.3 - Accumulator Input Logic Select

Function	Control Signal	Accumulator Input
Frequency A	B5	fa
Totalize	B5	fa
Ratio B	B8	fb
Frequency B	B8	fb
Period Average	B7	Reference frequency
Period	B6	Timebase
Time Interval	B6	Timebase
Time Interval Average	B10 (at TIA synchronizer)	GOSC

1.4.6 Differentiator

1.4.6.1 The signal selected by the counter input select logic is applied to the differentiator. The differentiator effectively shortens the duration of each pulse to limit the possibility of a signal occurring at the transition of the gate signal. This is accomplished as shown in figure 1.14. The selected input signal A and its delayed complement B are applied to an AND gate. The result is the very short duration pulse C whose width is equal to the propagation delay of the two gates in the delay circuit.

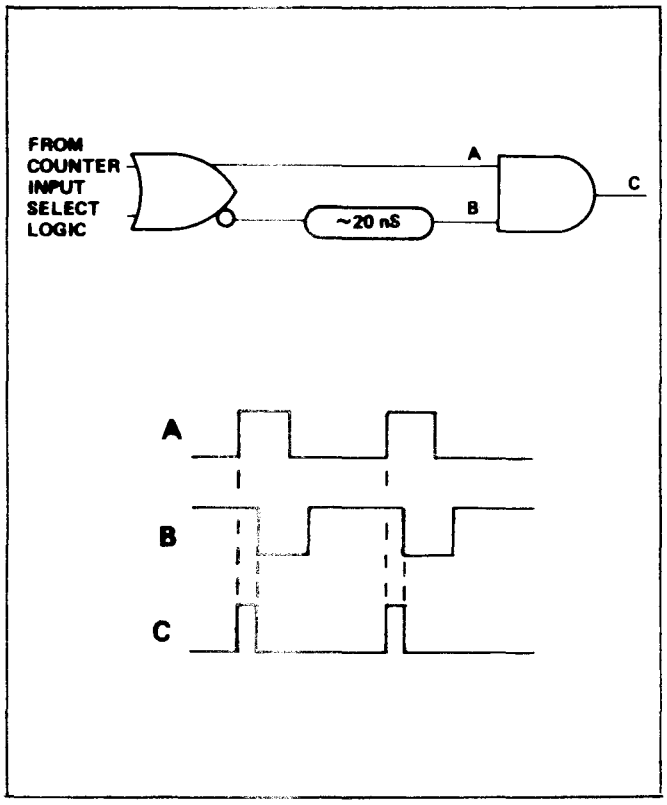


Figure 1.14 - Differentiator

1.4.7 Accumulator

1.4.7.1 The accumulator is a 9 digit BCD counter whose function is to count pulses during the time that the measurement gate remains open. A functional block diagram of the accumulator is shown in figure 1.15. The least significant digit displayed is counted by the ECL divider on the main board or by a 500 MHz divider located on the optional R.F. board depending on the function selected. Control signal B11 selects the BCD output from the R.F. board or from the 100 MHz ECL decade counter.

1.4.7.2 The output signal from the 100 MHz counter or the R.F. board carry output (depending on the function selected) is divided by 10 and then applied to the LSI7031 counter. This LSI circuit contains 6 decade counters and 8 latches together with multiplexing and timing circuits which allow it to interface directly to the display. Leading zero blanking logic is also internal to the chip. The carry output of the LSI7031 chip is divided by ten to form a ninth digit. The output from this 9th digit is fed back to the LSI7031 as the overflow input.

1.4.7.3 When the gate ends, the $\overline{\text{LOAD}}$ signal causes the BCD output from the counter to be latched. Beginning with the most significant digit in the LSI chip, each set of 4 lines of BCD data for each digit is strobed into the data buffer. An 8-state scan counter and decoder strobes the data into the output buffer and also to each digit of the display.

1.4.8 Display Logic

1.4.8.1 The display board contains the LED indicators and logic necessary to display nine digits of measurement data, a decimal point, unit annunciators, and GPIB interface status. To minimize the number of output lines between the accumulator and the display, the eight least significant digits are multiplexed. The display logic is shown in figure 1.18.

1.4.8.2 Four lines of BCD data (ST A, ST B, ST C, and ST D) from the LS7031 counter are applied to a BCD-to-7-line converter. The converter translates the binary coded decimal number and powers the appropriate segments of the LED indicator digit to represent the value. The BCD data applied to ST A through ST D is synchronized with strobes S1 through S8. Each strobe triggers a Darlington transistor driver connected to the anode to power the LED digit corresponding to the number coded on lines ST A through ST D.

1.4.8.3 The decimal point strobe sets the dp line high precisely at the time that the strobe signal occurs corresponding to the number on select code lines DP1, DP2, and DP4. For example, if the select code is 101, dp goes high with strobe signal S5. The decimal point driver is enabled at the same time that digit five data is on the data lines and the decimal point adjacent to digit five is illuminated.

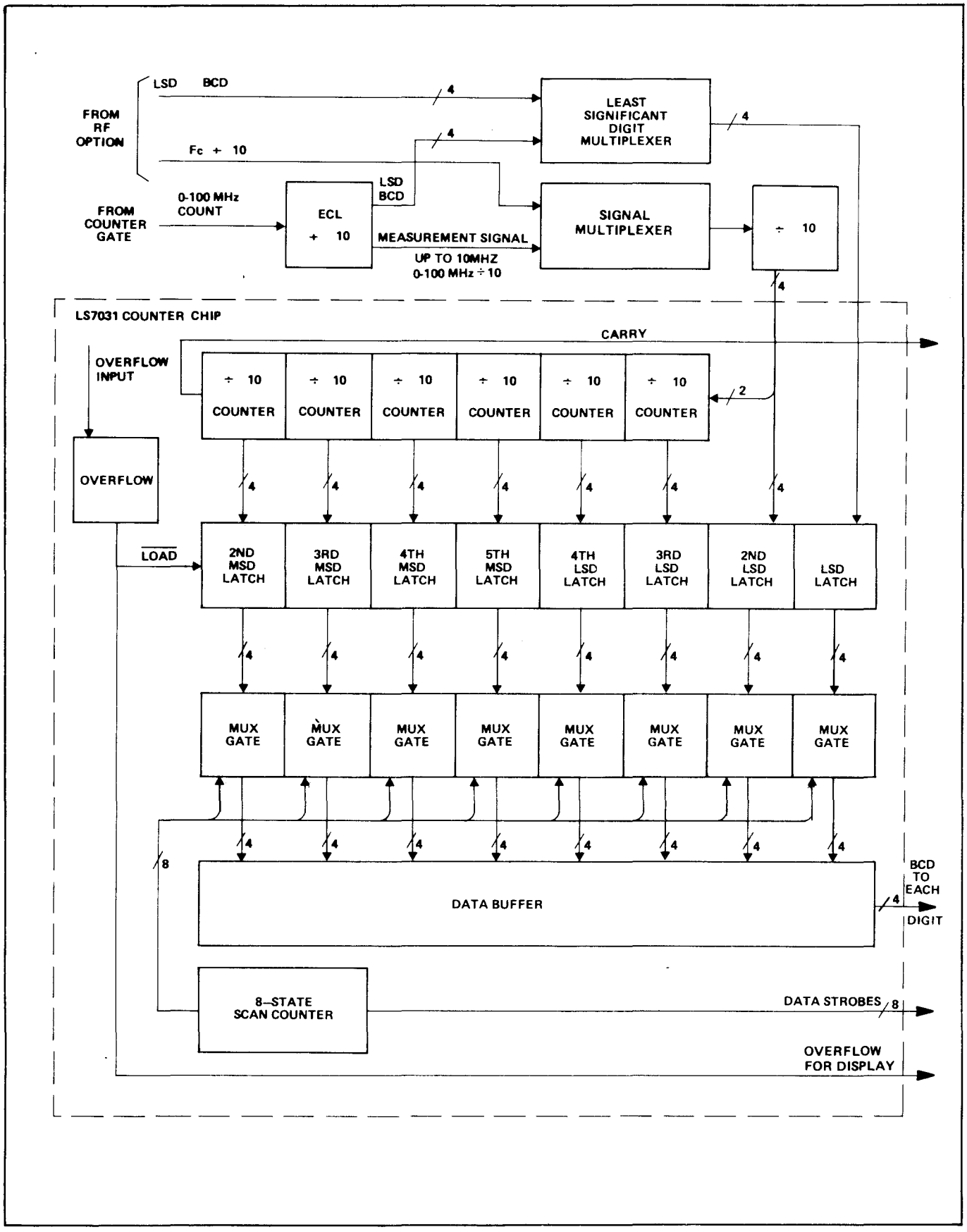


Figure 1.15 - Accumulator Functional Block Diagram

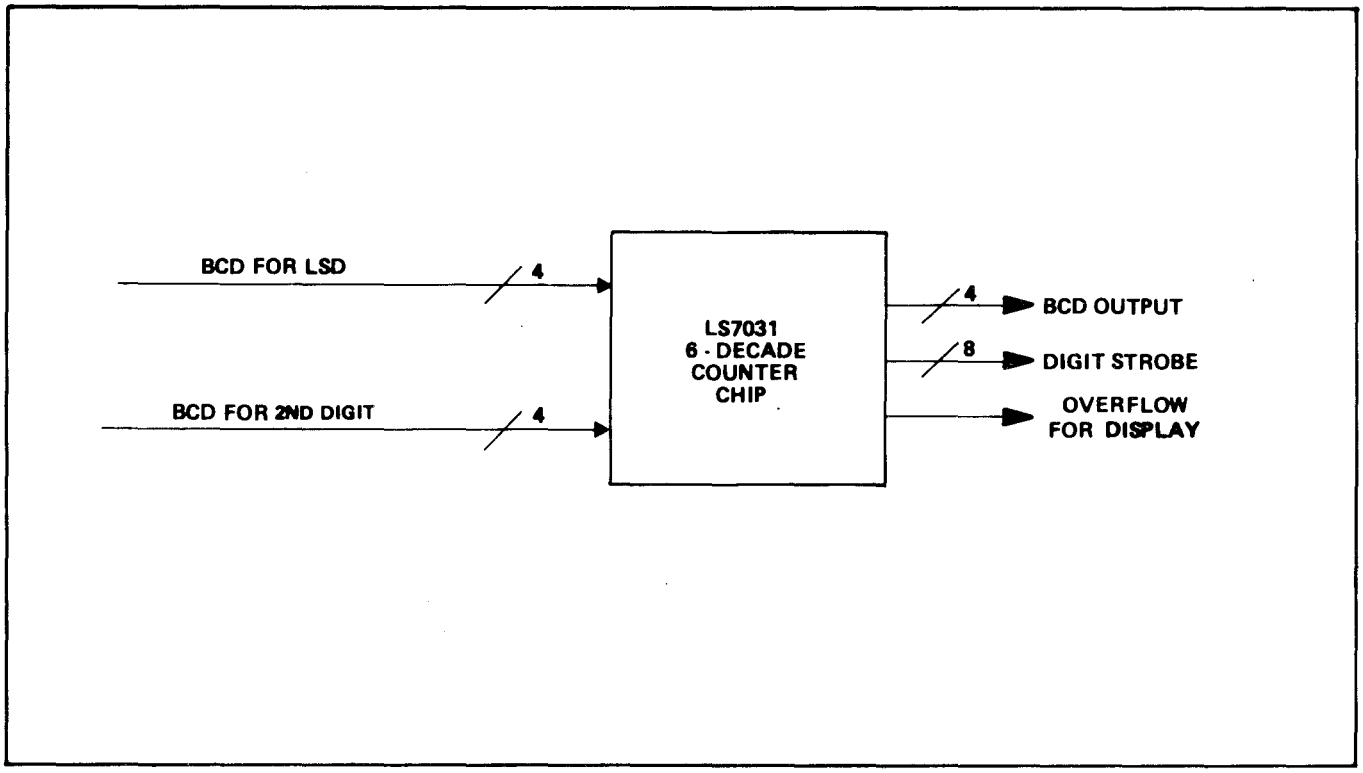


Figure 1.16 - Accumulator Data Flow

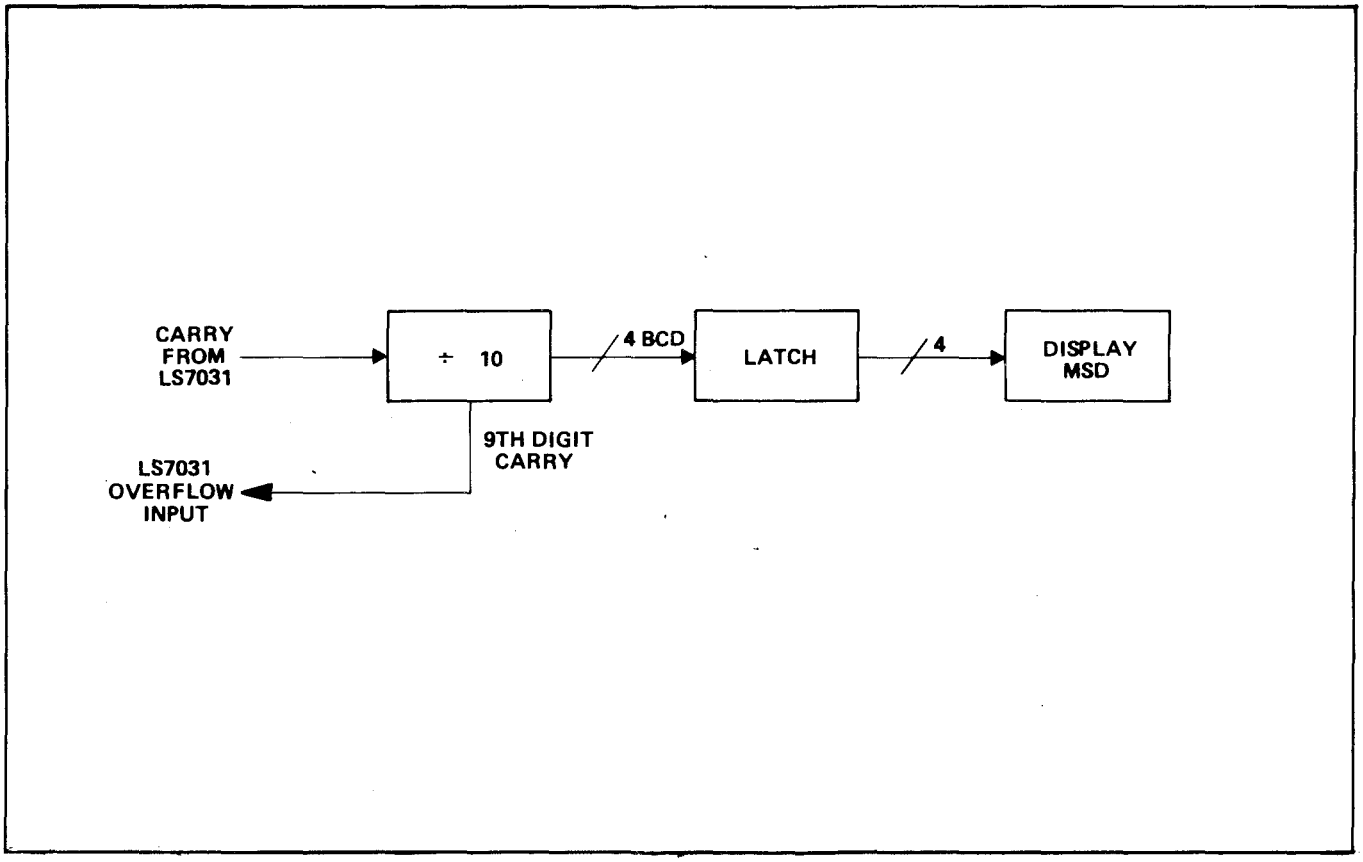


Figure 1.17 - Ninth Digit Data Flow

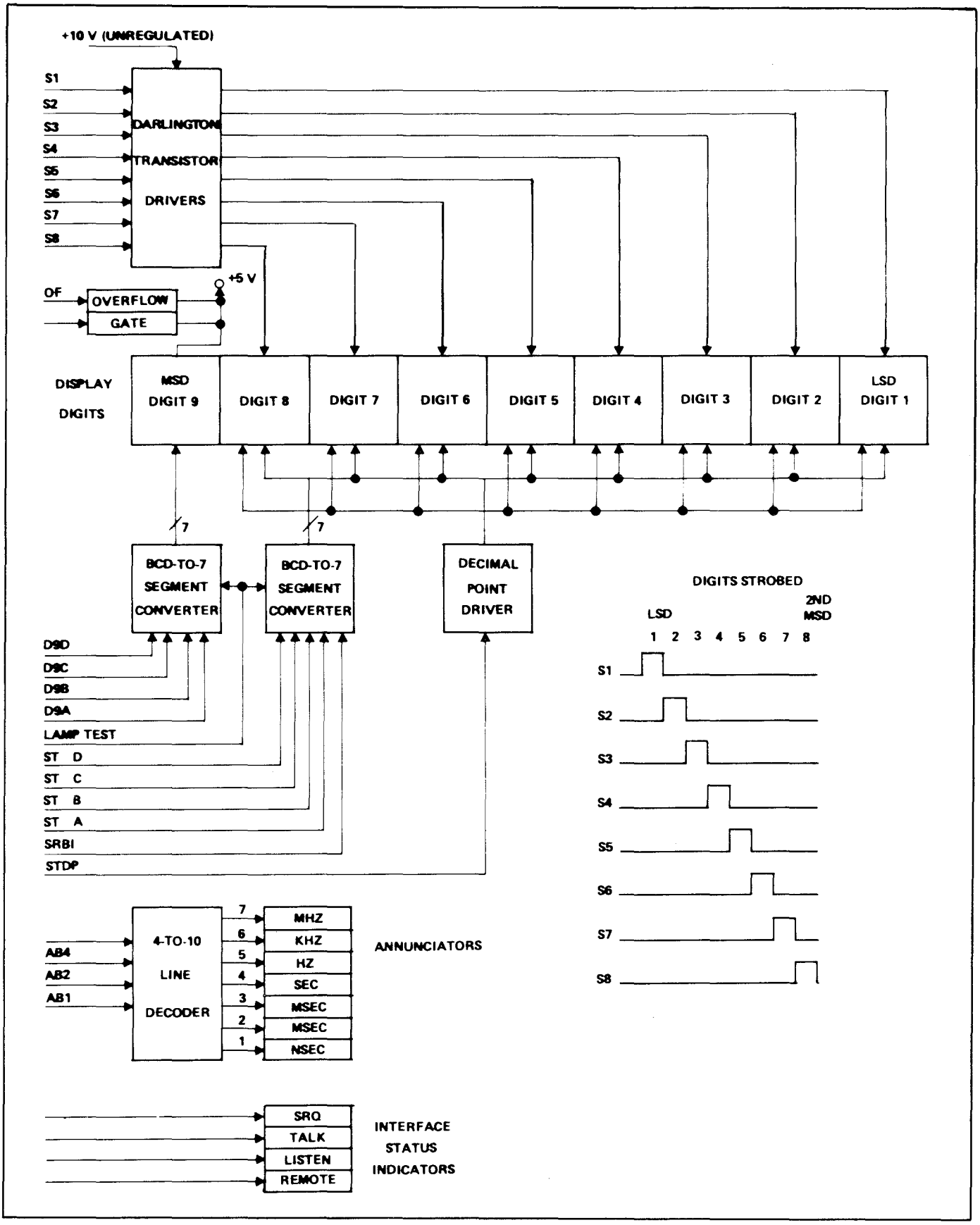


Figure 1.18 - Display Logic

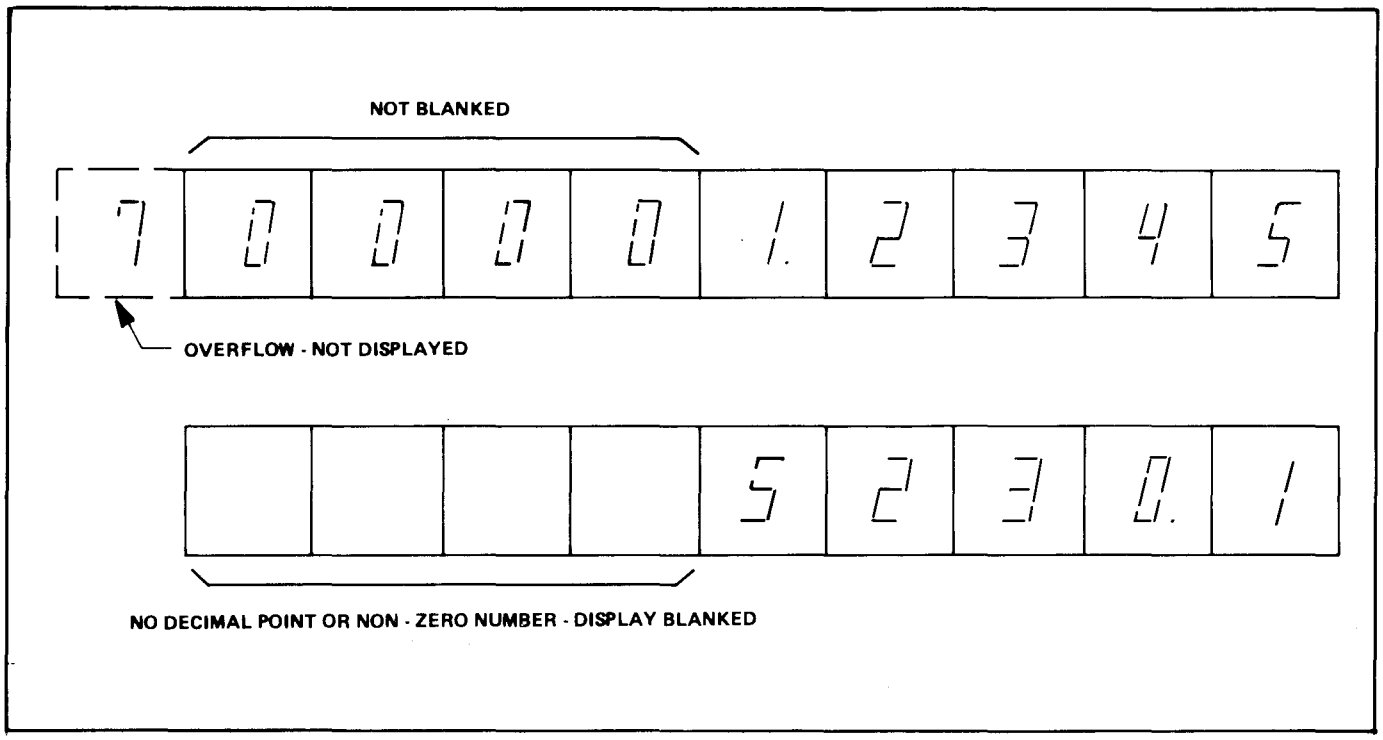


Figure 1.19 - Display Blanking

1.4.8.4 Display blanking occurs when no decimal point or digits other than zero are to the left of digits being counted in the LS7031 counter. When no decimal point or numbers are detected in the LS7031 counter, the strobed ripple blanking input signal (SRBI) is set high. SRBI is synchronized with the strobe lines. SRBI turns off the BCD-to-7-segment converter and no more digits are displayed even though the digits are still being strobed. SRBI is not set if an overflow exists even though the left hand digits are zero. See figure 1.19.

1.4.9 Timebase

1.4.9.1 The timebase divides its input signal by the factor selected by the N/RESOLUTION switch or the microprocessor (Model 9514) when the counter is under remote control. The timebase input signals are the 10 MHz reference signal, fa (TTL), $\overline{A \rightarrow B}$, control signals B2, B3, B6, RA, RB, RC, and ÷4. The output signal of the timebase is used in the gate control logic and the accumulator. A simplified logic diagram of the timebase is shown in figure 1.20.

1.4.9.2 The timebase consists of input select logic (TIMEBASE COUNTER CONTROL), a series of decade counters, and an 8-to-1 multiplexer. The input select logic is a 4-to-1 multiplexer used to gate the appropriate signal to the decade counters. See figure 1.21. Control signals B2, B3, and B6 select the output of the multiplexer. When the 1.25 GHz RF option is used, the multiplexer output is divided by four to compensate for the prescaling on the RF board. The ÷4 signal from the RF board enables the divide-by-four counter.

1.4.9.3 The 1 MHz signal is selected in the frequency measurement function. The effect is to make the shortest gate time (shortest opening of the gate) or output of the gate that is derived from the timebase 1 microsecond. The 1 MHz can also be divided down to yield a 10-second gate for a .1 Hertz resolution. The 1 MHz input is produced by dividing the 10 MHz reference signal by 10. See figure 1.20. The signal $\overline{A \rightarrow B}$ is used as an enable to the divide by 10 counter to make the opening of the gate synchronous with the input signal.

1.4.9.4 The 10 MHz reference signal is selected to provide a clock from 10 MHz down to 1 Hertz for period or time interval measurements with a maximum resolution of 100 nanoseconds. The 10 MHz reference signal is selected by control signal B6.

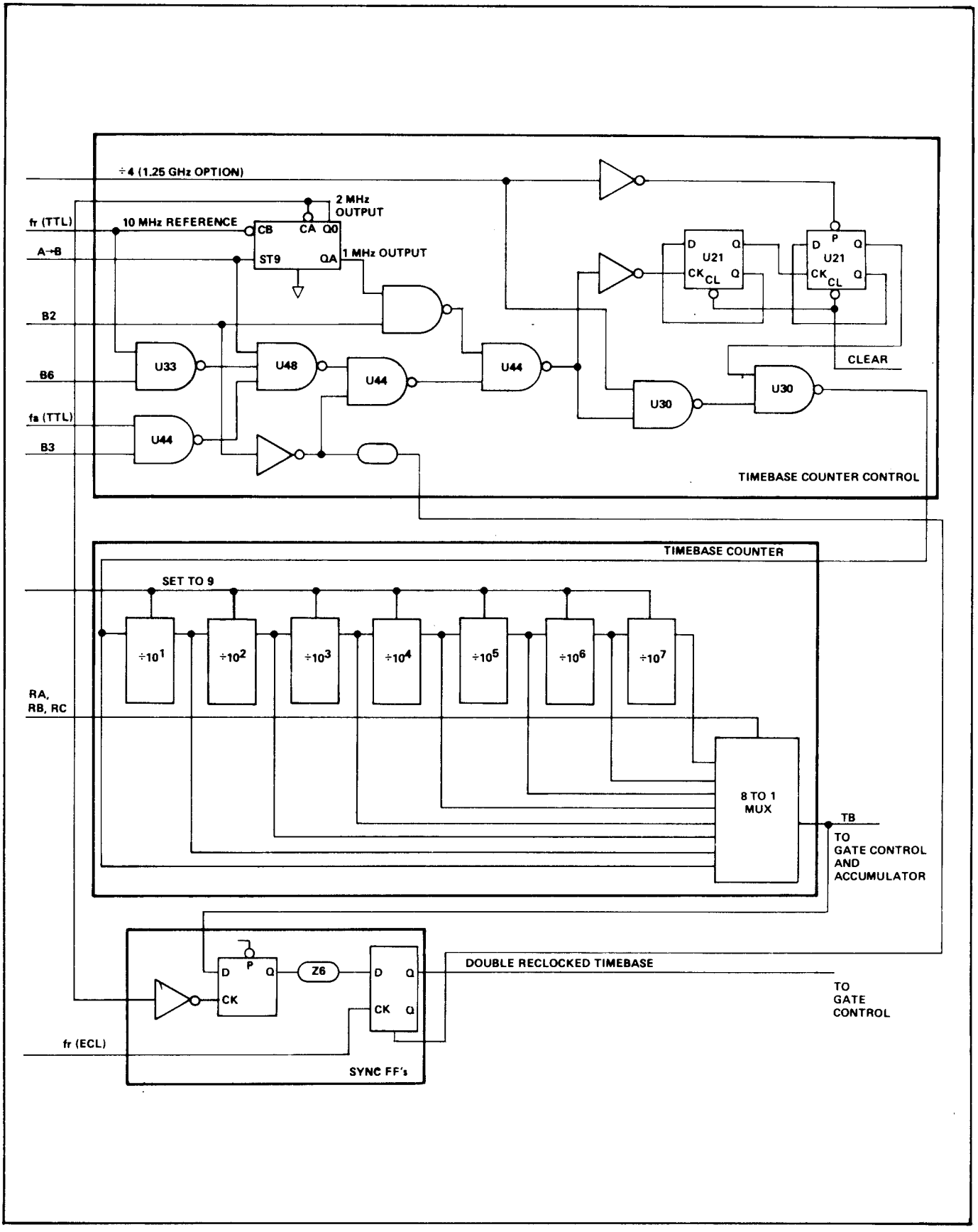


Figure 1.20 - Timebase Simplified Logic Diagram

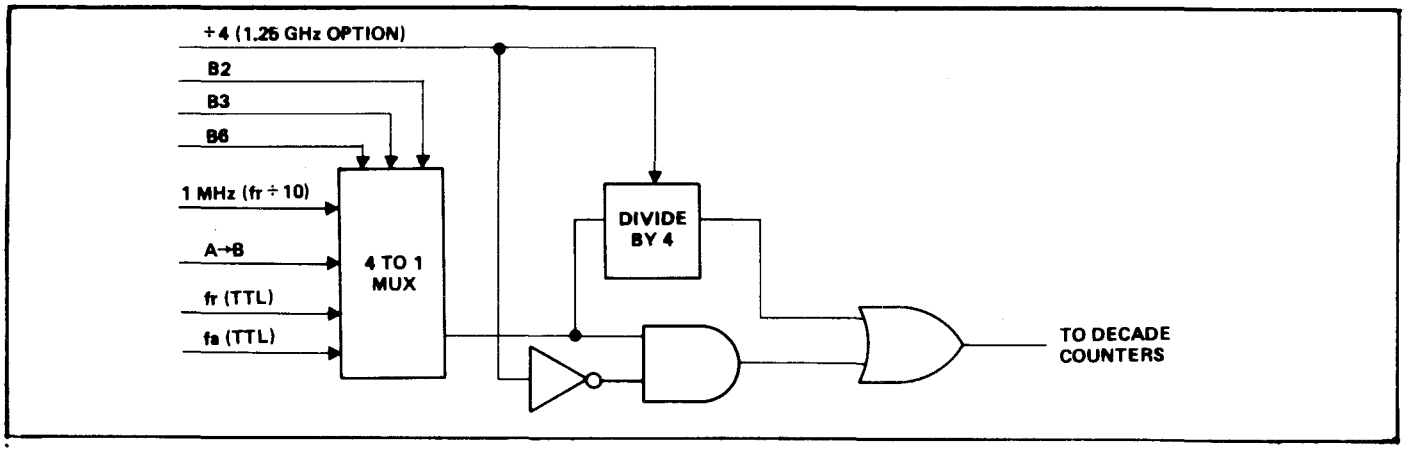


Figure 1.21 - Timebase Input Select Logic

1.4.9.5 The $\overline{A \rightarrow B}$ signal is used in time interval average measurements. This signal goes low on the channel A trigger and goes high on the channel B trigger. $\overline{A \rightarrow B}$ is generated in the TIA Synchronizer circuit and it is fed to the timebase dividers to keep track of the number of intervals being counted in the accumulator. The output of the timebase will be a decadic multiple of the signal $\overline{A \rightarrow B}$ and it is used to control the measurement gate.

1.4.9.6 The fa (TTL) signal is the measurement signal after the signal conditioning circuit and the ECL-to-TTL level translation. fa (TTL) is used for ratio and period average measurements and is limited to 10 MHz at this point by specification. The timebase dividers are used to generate a decadic multiple of the input signal period.

1.4.9.7 The timebase signal, after the input selection circuit, is applied to the 8-to-1 multiplexer directly from the series of seven divide-by-10 counters. Under control of the resolution select signals RA, RB, and RC, one of eight signals can be selected as an output of the timebase. The eight signals range from 10 MHz down to 1 Hertz. The control signal requirements for each output signal are listed in table 1.4. The timebase output is used in the accumulator, the gate control logic, and by the reclocking flip-flops.

Table 1.4 - Timebase Multiplexer Outputs

INPUTS			OUTPUTS		
RC	RB	RA	OUTPUT SELECTED	U41 PIN SELECTED	TIMEBASE FREQUENCY SELECTED*
L	L	L	0	4	10 MHz
L	L	H	1	3	1 MHz
L	H	L	2	2	100 kHz
L	H	H	3	1	10 kHz
H	L	L	4	15	1 kHz
H	L	H	5	14	100 Hz
H	H	L	6	13	10 Hz
H	H	H	7	12	1 Hz

* Time interval and period measurements only.

1.4.9.8 RECLOCKING THE TIMEBASE SIGNAL

1.4.9.8.1 The timebase signal is reclocked and synchronized with the 10 MHz reference signal to eliminate the uncertainties caused by propagation delays in the frequency measurement mode. In the worst case, the reference frequency is divided down from 10 MHz to 0.1 Hz in the timebase counters. The edge of each low frequency square wave can be within the uncertainty caused by the propagation delays in each gate of the divide-by-10-million chain. The maximum uncertainty allowed in order to stay within a ± 1 count roll-around is equal to less than one period of the maximum frequency to be measured which is 500 MHz. The reclocking method is diagrammed in figure 1.22.

1.4.9.8.2 The uncertainty is eliminated by clocking the output of the timebase with the reference oscillator divided by five. The reference oscillator signal is not used directly because of the chance of missing one full period of the signal which would compound the uncertainty instead of eliminating it. The first stage of the reclocking is to reduce the uncertainty of the edges of the timebase output down to that of the TTL flip-flop. The signal is then translated to an ECL level and reclocked directly with the reference oscillator signal. The signal is kept at ECL logic levels so that the uncertainties caused by propagation delays are much lower. The output of this circuit is DRTB (double reclocked timebase) and is used by the measurement gate input control circuit in the frequency measurement functions.

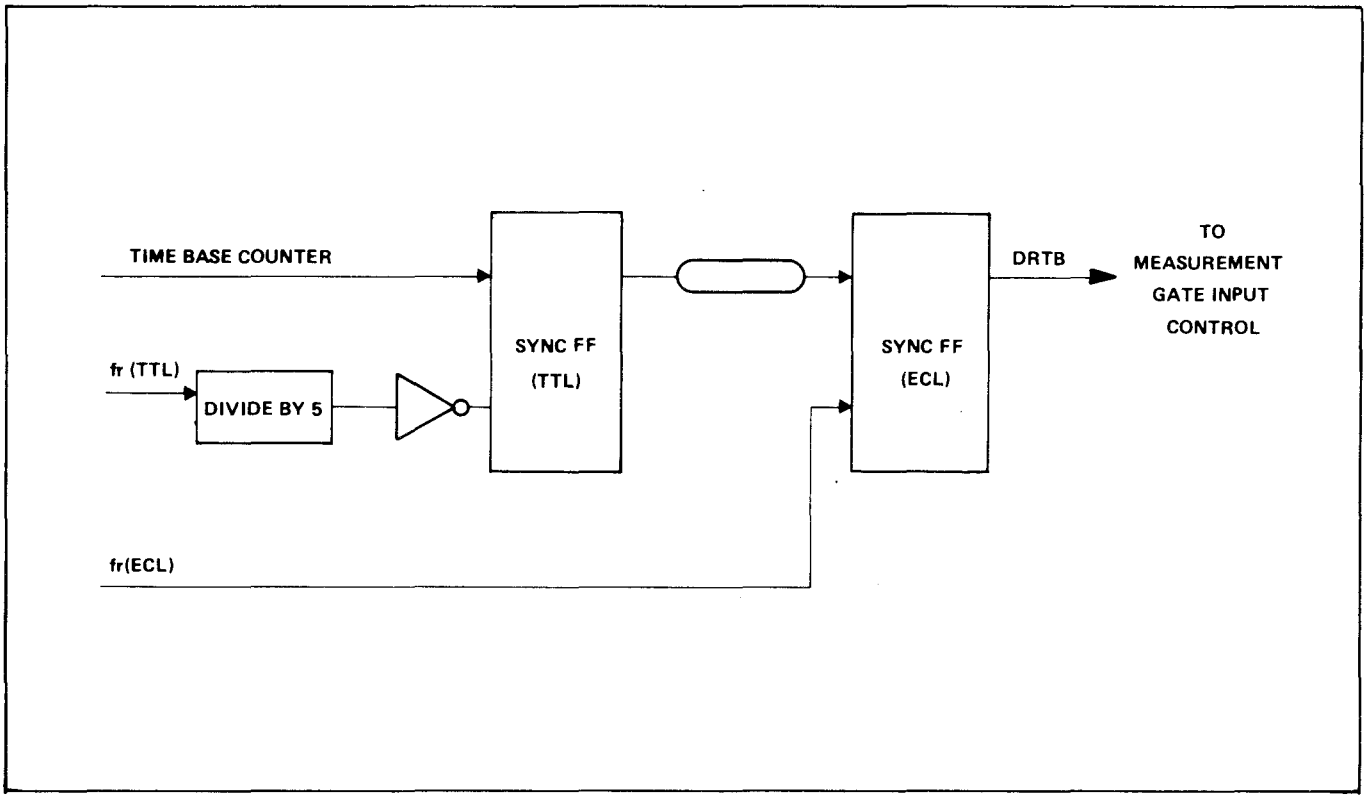


Figure 1.22 - Timebase Synchronizing

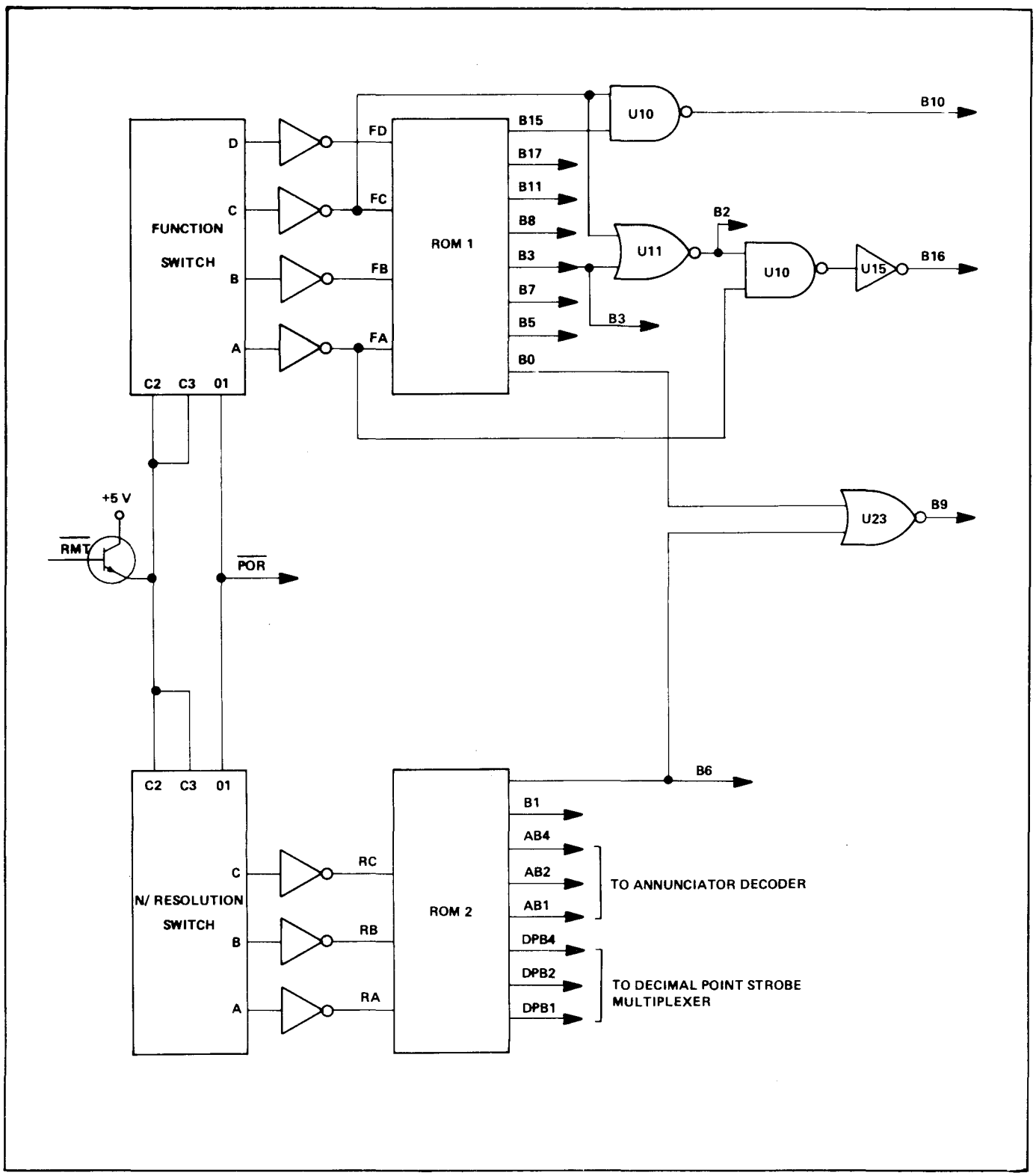


Figure 1.23 - Function and Resolution Logic

1.4.10 Function and Resolution Select

1.4.10.1 The function and resolution logic determine which circuits within the counter are activated. Figure 1.23. shows the function and resolution logic. The function and resolution logic is contained in read-only memory (ROM) and addressed by the front panel FUNCTION and N/RESOLUTION switches in local control or by the microprocessor (Model 9514 only) in remote control.

1.4.10.2 The FUNCTION and N/RESOLUTION switches each have three wafers. Wafer 01 is used only shorted to ground during switching to clear the counter and prepare for the new function. This is accomplished by setting the power on reset signal (POR) momentarily low.

1.4.10.3 Wafers C2 and C3 of the FUNCTION and N/RESOLUTION switches are enabled by the $\overline{RMT}$ signal being high. Not being in remote control, grants control locally to the front panel switches. $\overline{RMT}$ turns on transistor Q3 and applies +5 volts to wafers C2 and C3.

1.4.10.4 In the extreme counterclockwise position (F_A-FUNCTION switch, 0 1 MHz, N/$\overline{RESOLUTION}$ switch) of each switch, output pins $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$ are pulled up to the +5 volts on C2 and C3. $\overline{A}$, $\overline{B}$, $\overline{C}$ and $\overline{D}$ are inverted through U14 and U15 applying all zeros to the read-only memories ROM1 and ROM2. Signals FA, FB, FC, and FD for ROM1 and RA, RB, and RC for ROM2 provide the address or control signals in local control. Because inverters U14 and U15 are open-collector gates, FA, FB, FC, FD, RA, RB, and RC can be provided remotely over the GPIB. Each position of the FUNCTION and N/RESOLUTION switches sets up a unique combination of inputs to the ROM's and thereby produce a unique output. The output signals generated for each input combination of the FUNCTION switch are listed in table 1.5.

Table 1.5 - Control ROM Outputs

* = Don't care 0 = Low 1 = High B4 and B13 Not used					Circuit Controlled														
					Gate	Gate	Gate Timebase	Timebase	Accumulator	Accumulator Timebase	Accumulator	Accumulator	Accumulator	Synchronizer	RF Board Synchronizer	Synchronizer	Gate	Synchronizer	Signal Conditioner	Signal Conditioner
Function	ROM INPUT																			
	FD	FC	FB	FA	B0	B1	B2	B3	B5	B6	B7	B8	B9	B10	B11	B12	B14	B15	B16	B17
F_A	0	0	0	0	*1	*0	1	*0	0	0	0	1	0	1	0	0	1	1	0	1
F_C	0	0	0	1	*1	*0	1	*0	1	0	0	1	0	1	1	0	1	1	1	*
R_B	0	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1
R_C	0	0	1	1	1	1	0	1	1	0	0	1	0	1	1	0	1	0	0	1
P	0	1	0	0	1	0	0	0	1	1	0	1	0	1	0	0	1	0	0	1
TI	0	1	0	1	0	0	0	0	1	1	0	1	0	1	0	0	1	0	0	0
PA	0	1	1	0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	0	1
TIA	0	1	1	1	1	1	0	0	1	0	0	1	0	0	0	0	1	1	0	0
F_B	1	0	0	0	*1	*0	1	*0	1	0	0	0	0	1	0	1	1	1	0	1
C/A→B	1	0	0	1	0	0	0	*1	1	0	0	1	1	1	1	*1	1	0	0	0
TOT	1	0	1	0	0	1	0	*1	0	0	0	1	1	1	0	*1	0	0	0	1
ATA	1	1	1	0	*1	*	0	*	0	0	0	1	0	*	*	*1	1	*	0	0
ATB	1	1	1	1	*1	*	0	*	1	0	0	0	0	*	*	*1	1	*	0	0

(ATA and ATB used during AUTO TRIGGER.)

1.4.10.5 For each position of the FUNCTION and N/RESOLUTION switches, control signals B0 through B17 are generated to activate the circuit required to perform the function of the desired resolution. An asterisk indicates that the circuit listed is not required for the corresponding function.

1.4.10.6 In addition to the control ROM outputs signals, some control signals are a result of the combination of others. The combination control signals are listed in table 1.6.

Table 1.6 - Combination Control Signals

Signal Generated	Signals Required	Gate
B2	FC low and B3 low	U11
B9	B0 low and B6 low	U23
B10	FC low or B15 low	U10
B12	FD high	None
B14 (TO)	FB low or B9 low	U4
B16	FA high and B2 high	U10

1.4.10.7 The octal select codes for the annunciators and the decimal point are also generated in ROM2. The annunciator bits AB1, AB2, and AB4 are applied to the 4-to-10 line decoder on the display board to indicate the units of measure of the displayed measurement. The annunciator illuminated for each octal select code is listed in table 1.7. The octal select code for the decimal point is applied to the decimal point strobe to illuminate the decimal point indicator.

Table 1.7 - Annunciator Select Code

Octal Select Code			Annunciator
AB4	AB2	AB1	
0	0	1	nsec
0	1	0	μsec
0	1	1	msec
1	0	0	sec
1	0	1	Hz
1	1	0	kHz
1	1	1	MHz

1.4.11 Measurement Gate (Main Gate)

1.4.11.1 The measurement gate is enabled by the GATE pulse. The duration of the GATE pulse is determined by the setting of the front panel N/RESOLUTION switch. The counter's main gate transfers pulses from the differentiator to the accumulator for the precise amount of time set by the N/RESOLUTION switch or the remote controller. The time settings corresponding to each position of the N/RESOLUTION switch are listed in table 1.8.

Table 1.8 - Gate Time

Sw Pos	Resolution in F_A, F_B, F_C	No. of Periods of Channel A Signal PA, C/A, B/A	Resolution in P, T1	F_A, F_B, F_C Gate Time	Number of Intervals Averaged in TIA
0	1 MHz	$10^0 = 1$	.1 usec	1 usec	1
1	.1 MHz	$10^1 = 10$	1 usec	10 usec	10
2	10 kHz	$10^2 = 100$	10 usec	100 usec	100
3	1 kHz	$10^3 = 1{,}000$	.1 msec	1 ms	1000
4	.1 kHz	$10^4 = 10{,}000$	1 msec	10 ms	10,000
5	10 Hz	$10^5 = 100{,}000$	10 msec	100 ms	100,000
6	1 Hz	$10^6 = 1{,}000{,}000$	.1 sec	1 sec	1,000,000
7	.1 Hz	$10^7 = 10{,}000{,}000$	1 sec	10 sec	10,000,000

1.4.12 Measurement Gate Input Control

1.4.12.1 The measurement gate input control circuit selects a signal to open and close the measurement gate. The measurement gate input control is comprised of two channels, one for start and one for stop. One of the five input signals to the gate control input select, $\overline{fa}$, $\overline{fb}$, $\overline{s/s}$, TB, and DRTB can be applied to either or both channels of the gate control. The same signal may be used to both start and stop the gate, or two separate signals may be used to start and stop the gate.

1.4.12.2 Four of the input signals are applied to a dual four-to-one multiplexer in each channel. See figure 1.24. The multiplexers that select the signals for starting and stopping the gate are under control of signals B0 and B1 (reference table). In the frequency measurement modes, the dual 4-to-1 is disabled by B2 and the signal DRTB is activated to provide the gate timing. The signals selected to start and stop the gate are applied to the clock inputs of the start and stop flip-flops respectively. The rising edge of both start and stop signals are used to keep propagation differences to a minimum.

1.4.12.3 The signal from the $\overline{Q}$-output of the start flip-flop is used to open the gate. See figure 1.25. The stop signal is taken from the Q-output to close the gate.

1.4.12.4 The two outputs of the gate control are $\overline{GATE}$ which is the actual measurement gate control and its inverted signal to the gate buffering circuit. The buffering circuits are involved in the timing between measurements. $\overline{GATE}$ is buffered, inverted, and supplied to the rear panel GATE OUT BNC jack for external use.

1.4.12.5 The gate delay signal overrides the stop signal and keeps the gate open. GDY keeps the stop flip-flop reset to prevent the counter from closing the gate. The gate delay signal is supplied by the user through a rear panel BNC.

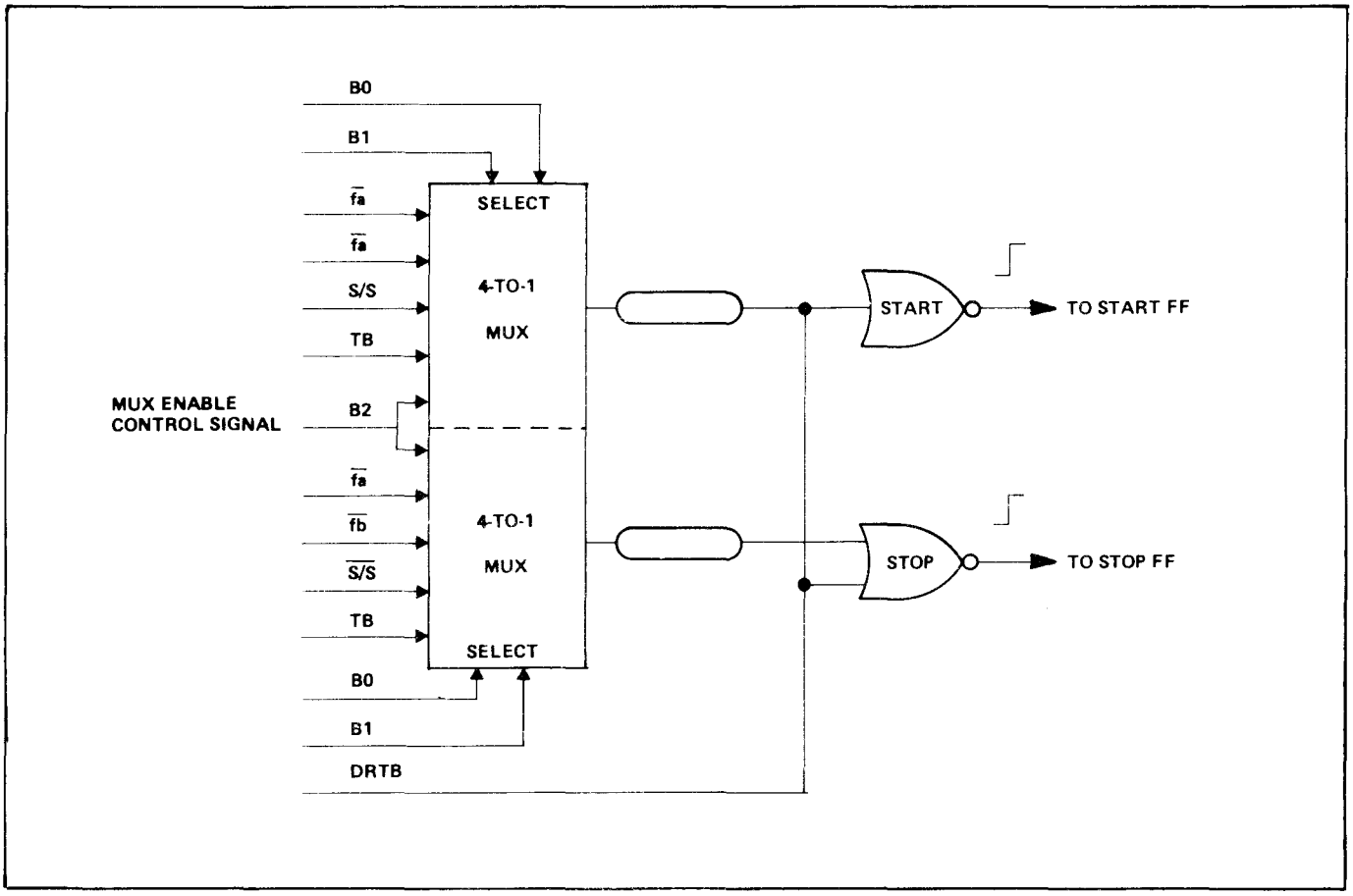


Figure 1.24 - Measurement Gate Input Control

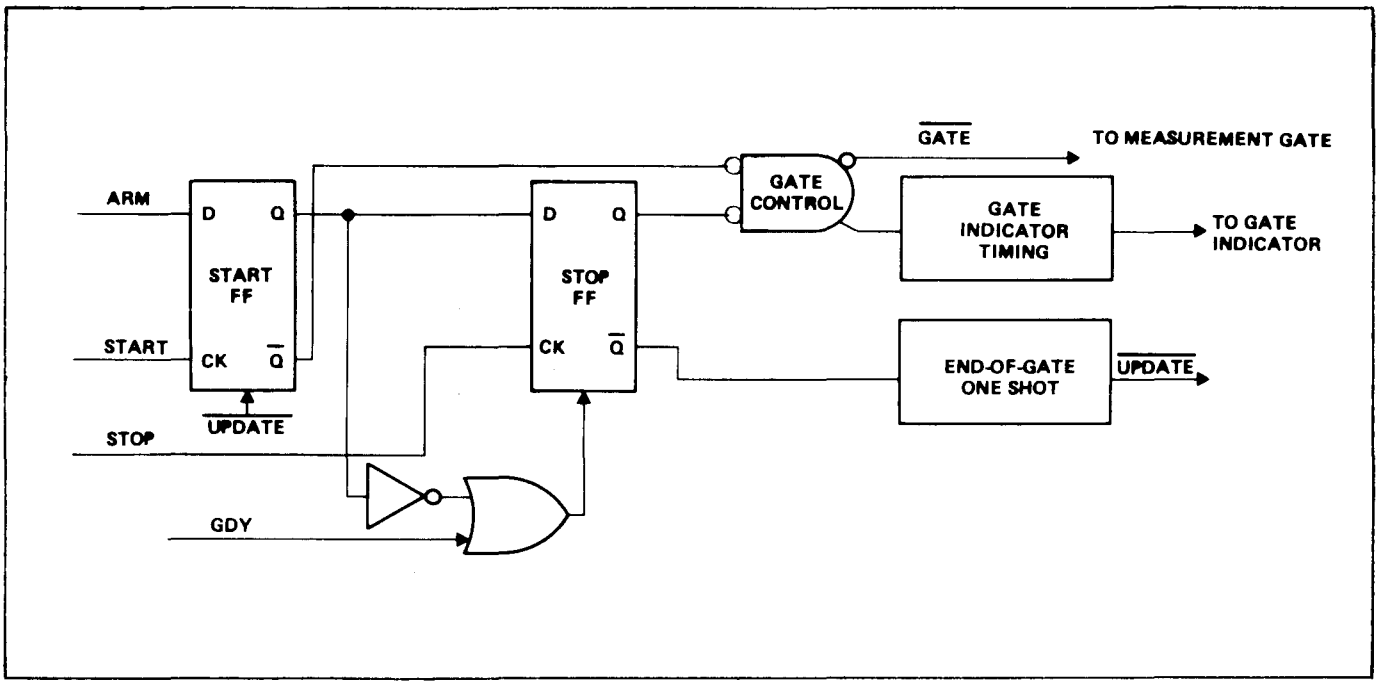


Figure 1.25 - Measurement Gate Control Logic

1.4.12.6 The start flip-flop is reset by the $\overline{\text{UPDATE}}$ signal. $\overline{\text{UPDATE}}$ occurs at the end of the measurement cycle and loads the measurement into the display.

1.4.12.7 ARM is applied to the D-input of the start flip-flop and it is clocked through by the start signal. The $\overline{\text{Q}}$-output is used to open the gate. The Q-output of the start flip-flop is applied to the D-input of the stop flip-flop and is also inverted and applied to the reset input of the stop flip-flop. These connections guarantee that the stop flip-flop will not react to a stop signal until the gate has opened.

1.4.13 Gate Arming Control

1.4.13.1 The gate arming control flip-flop arms or prepares the start flip-flop to open the measurement gate. This is accomplished by a high ARM signal being applied to the D-input of the start flip-flop. The ARM signal is developed from the external arm enable local ($\overline{\text{EAEL}}$) signal, external arm enable remote ($\overline{\text{EAER}}$) signal from the GPIB, or from the $\overline{\text{CLEAR}}$ signal. See figure 1.26. When the GPIB is not being used ($\overline{\text{EAER}}$) and the rear panel input is not being used ($\overline{\text{EAEL}}$), the $\overline{\text{CLEAR}}$ signal generates the ARM signal. The NAND gates of U31 form a two-to-one multiplexer to select the $\overline{\text{CLEAR}}$ signal. With both $\overline{\text{EAER}}$ and $\overline{\text{EAEL}}$ high, the inverted output of NAND gate U27 enables U31A. $\overline{\text{CLEAR}}$ is gated through U31A and U32 since the external arm (EA) signal is holding U31B output high. ARM clocks the gate arming flip-flop to set the D-input of the start flip-flop high and thereby arming it.

1.4.13.2 When either $\overline{\text{EAER}}$ or $\overline{\text{EAEL}}$ is low, the inverted high output of U27 prevents the $\overline{\text{CLEAR}}$ signal from being gated through U31A but sets the D-input of the external arm flip-flop high. The rising edge of the CLEAR signal generates a high level through the external arm flip-flop. The rising edge of EA is inverted through U31B and again through U32 to clock the gate arming control flip-flop and set the D-input of the start flip-flop high. The $\overline{\text{Q}}$-output of the gate arming control flip-flop resets the external arm flip-flop.

1.4.13.3 The gate arming control is disabled in the totalize function. In the totalize function, start and stop of the gate is controlled by the front panel START/STOP switch. The totalize signal, $\overline{\text{TO}}$, holds the gate arming flip-flop in the set state and overrides the $\overline{\text{UPDATE}}$ clear signal that normally occurs at the end of the measurement cycle.

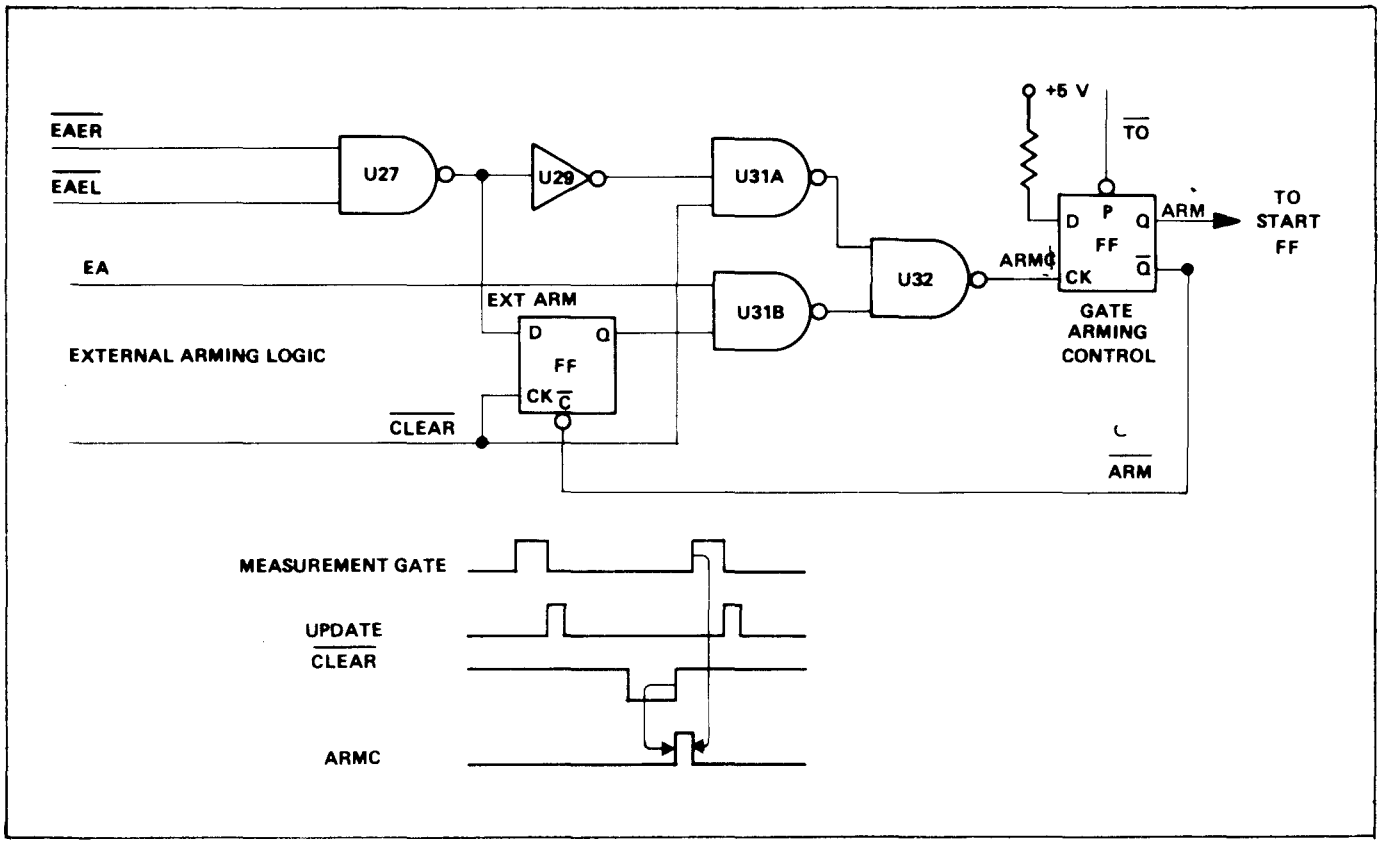


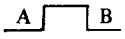
Figure 1.26 - Gate Arming Logic and Timing Diagram

1.4.14 Gate Control Signal Conditioner

1.4.14.1 The gate control signal conditioner selects the external gate control mode of operation and the signals to arm the measurement gate. A simplified logic diagram of the gate control signal conditioner is shown in figure 1.27. The rear panel arming mode switch has three positions. The signals activated by the arming mode switch are listed in table 1.9. The selective gate position causes the counter to arm on the leading edge of the external gate signal and to allow the closing of the gate or the trailing edge of the external gate signal. The measurement gate opens on the first start signal following the leading edge of the external gate signal. The measurement gate closes on the first stop signal following the trailing edge of the external gate signal.

1.4.14.2 The gate delay position causes the measurement gate to remain open until the external control gate goes low.

Table 1.9 - Arming Mode Switch Positions

Arming Mode Switch Position	Physical Position	Signals Activated
Selective Gate 	Left	$\overline{GDL}$, $\overline{EAEL}$
Gate Delay	Center	$\overline{GDL}$
Synchronous Window 	Right	$\overline{SWL}$

1.4.14.3 The synchronous window position is used to select a portion of a waveform to analyze. The synchronous window is only used with the time interval average function or auto trigger and causes the counter to see only the part of the input signal bracketed by the control waveform. This is accomplished by keeping the synchronizer in the preset state, and by disabling the inputs to the auto trigger latches whenever the external control state is low.

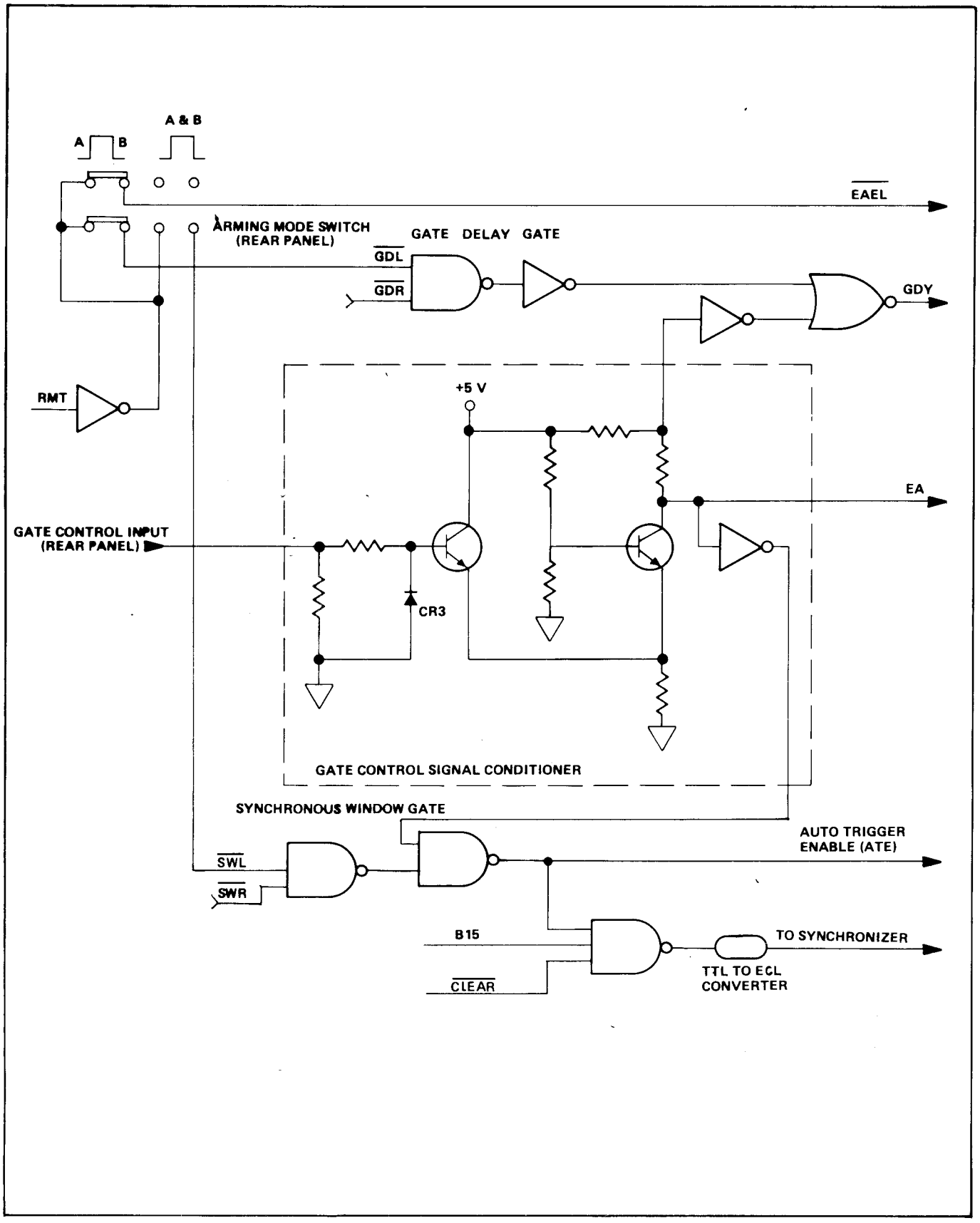


Figure 1.27 - Gate Control Simplified Logic Diagram

1.4.14.4 In the selective gate position, the gate delay local ($\overline{GDL}$) signal and the external arm enable local ($\overline{EAEL}$) signal are set low through the rear panel arming mode switch. GDL is inverted through the gate delay NAND gate and again through the inverter to enable the gate delay NOR gate. The gate delay (GDY) signal can then be controlled by an external signal applied to the GATE CONTROL input. The rising edge of the external signal causes the input transistor to conduct and produces a high TTL-level signal on external arm (EA). An inverted ECL-level holds GDY high and keeps the stop flip-flop in the reset position. The falling edge of the external gate control input signal will lift the GDY reset condition of the stop flip-flop and allow the gate to close.

1.4.14.5 In the synchronous window position, $\overline{SWL}$ is set low by the switch or $\overline{SWR}$ is set low by the remote interface (Model 9514 only). This allows the external control gate to pass through to the auto-trigger latches. The auto trigger latches are enabled whenever the ATE signal is high. The synchronizer is also enabled by the same signal.

1.4.15 Reset Logic

1.4.15.1 The reset logic initializes conditions in the counter. A simplified logic diagram of the reset logic is shown in figure 1.28. The reset logic generates the CLEAR signal to clear the accumulator, generates the DRES signal to load zeros into the display, and sets all nines in the time base counter. The RESET signal has three sources:

1. Power on reset – $\overline{POR}$
2. RESET SWITCH – $\overline{RES}$
3. FUNCTION-N/RESOLUTION switches – $\overline{POR}$

1.4.15.2 POWER ON RESET

1.4.15.2.1 When power is initially applied to the counter, the +5 volts slowly charges capacitor C1 keeping NAND gate U4 input from reaching the triggering threshold until other logic has had a chance to stabilize. NAND gate U4 and inverter U15 form a Schmitt trigger circuit so that the slowly rising input will not cause oscillations throughout the counter. The Schmitt trigger output remains low until the input reaches the threshold. While U15 pin 2 is low, the RESET signal at TP3 is high. Since $\overline{RMT}$ is also high, the data reset ($\overline{DRES}$) signal is low. $\overline{DRES}$ generates the $\overline{LOAD}$ signal to load zeros into the display. The Schmitt trigger output also holds NAND gate U27A output high which is inverted in U27B and reinverted through U27C. At test point TP6, CLEAR is produced to clear the accumulator.

1.4.15.2.2 As the Schmitt trigger reaches the triggering threshold, the output at U15 pin feeds back to the input and causes U4 to cross the threshold rapidly and eliminate the possibility of oscillations. The Schmitt trigger is also used to cause the logic to be reset when changing the setting of the FUNCTION and N/RESOLUTION switches.

1.4.15.3 RESET SWITCH

1.4.15.3.1 The RESET switch performs three functions:

1. Generate the reset signal – $\overline{RES}$.
2. Generate the lamp test signal – $\overline{LT}$.
3. Send the return to local control signal RTL to the interface (Model 9514 only).

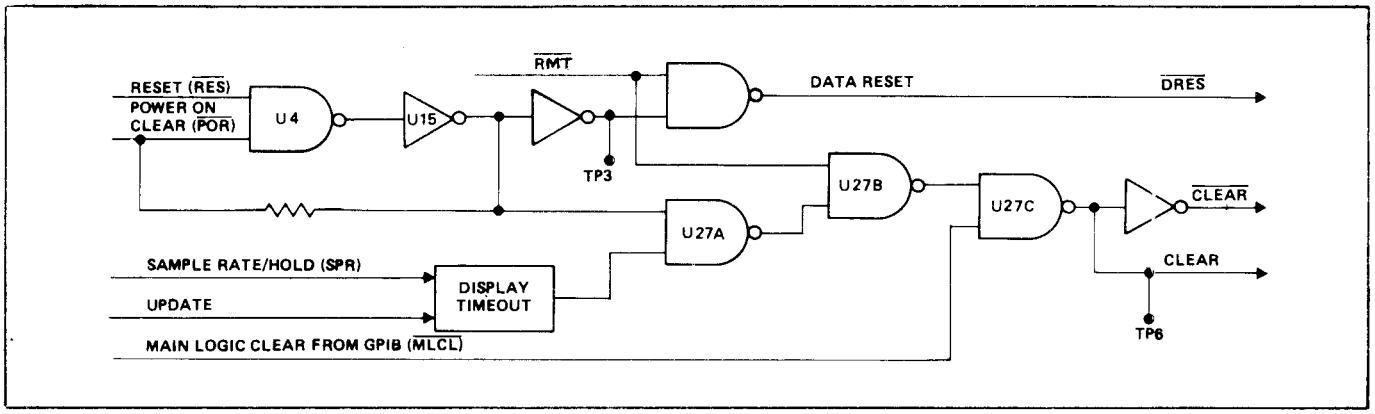


Figure 1.28 - Reset Logic Simplified Diagram

1.4.15.3.2 When the RESET switch is pressed, $\overline{RES}$ is generated through U4. $\overline{RES}$ fires the Schmitt trigger and sets RESET high through inverter U15. The RESET switch has the same effect as the power-on signal. Holding the RESET switch, grounds the lamp test signal $\overline{LT}$ and lights all of the segments of the display.

1.4.15.3.3 If the counter is in remote control, pressing the RESET switch generates the request for return to local control (RTL). RTL returns control of the counter to front panel switches if the microprocessor has not been instructed to ignore such requests.

1.4.16 Update

1.4.16.1 The $\overline{UPDATE}$ signal is initiated by the stop signal of the measurement gate. A simplified diagram of the update circuit is shown in figure 1.29. The update signal loads the contents of the accumulator into the display and starts the display timeout circuit to display the measurement data long enough to be read by the user. At the end of the display timeout the CLEAR signal is generated and a new measurement cycle is started. See figure 1.29.

1.4.16.2 When the stop flip-flop $\overline{Q}$-output is inverted through transistor inverter Q10, the 50 microsecond one shot multivibrator fires and generates the $\overline{UPDATE}$ signal at test point TP10. $\overline{UPDATE}$ clears the arm flip-flop through U33 and U25 and resets the start flip-flop through U32. The START signal is inverted through U49 to reset the stop flip-flop and set the $\overline{Q}$-output high again. $\overline{UPDATE}$ would be a very short pulse if not stretched to 50 microseconds by the one-shot multivibrator. Inverted through NAND gate U13, $\overline{UPDATE}$ is again inverted through NOR gate U11 to produce $\overline{LOAD}$. $\overline{LOAD}$ is applied to the LS7031 counter to load data from the accumulator to the display. $\overline{UPDATE}$ is also applied to the display timeout circuit and the data ready flip-flop. See figure 1.30. The time constant of the SAMPLE RATE/HOLD potentiometer on the front panel, resistor R90, and capacitor C45 determines the length of time that each measurement is displayed. The measurement gate cycle timing diagram is shown in figure 1.31. The output signal of the display timeout circuit goes to the reset logic to generate the CLEAR signal. When $\overline{UPDATE}$ sets the data ready flip-flop, the Q-output is set low to generate the data ready signal ($\overline{DRDY}$) to the GPIB (Model 9514).

1.4.17 TIA Synchronizer

1.4.17.1 The TIA sychronizer circuit enables the averaging the ± 1 count uncertainty of a time interval measurement over a decadic number of time intervals to achieve resolutions greater than 100 ns with repetive signals. Shown in the simplified diagram of figure 1.32, the TIA synchronizer is mainly impleted in ECL logic. The number of time intervals averaged is determined by feeding the signal $\overline{A \rightarrow B}$ into the time base generator and its output used to control the main measurement gate.

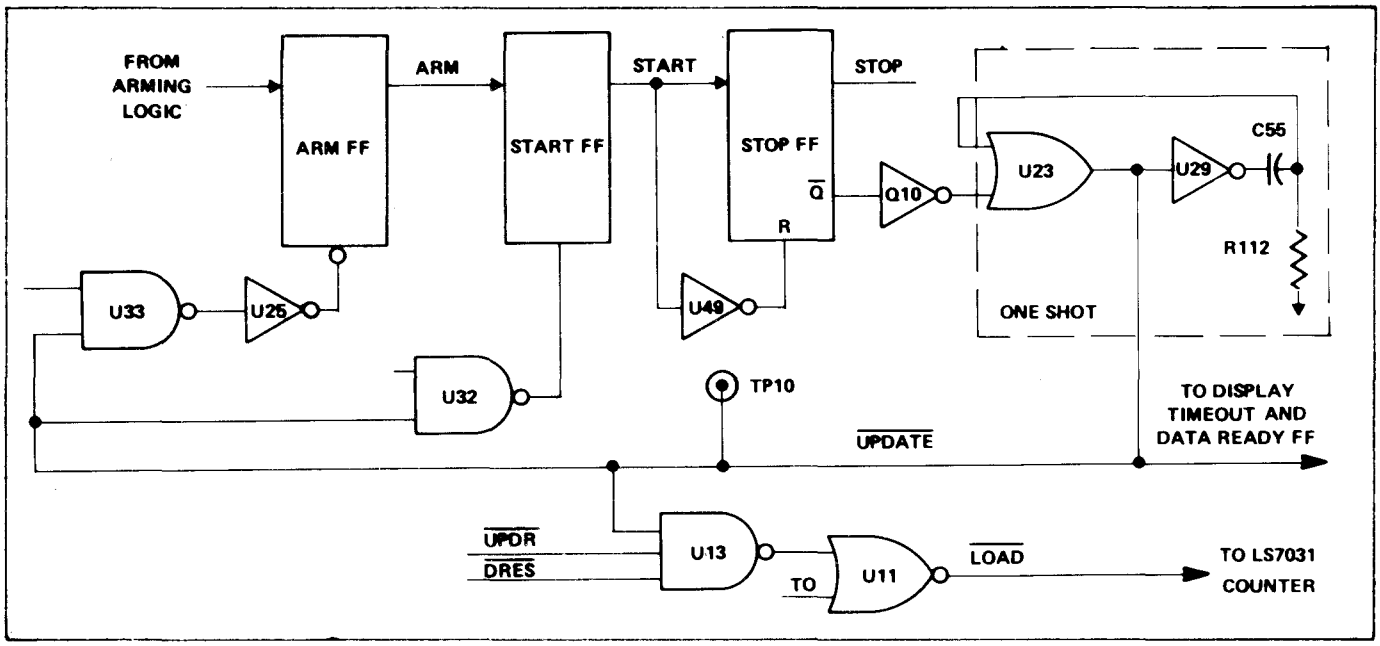


Figure 1.29 - Update Simplified Logic Diagram

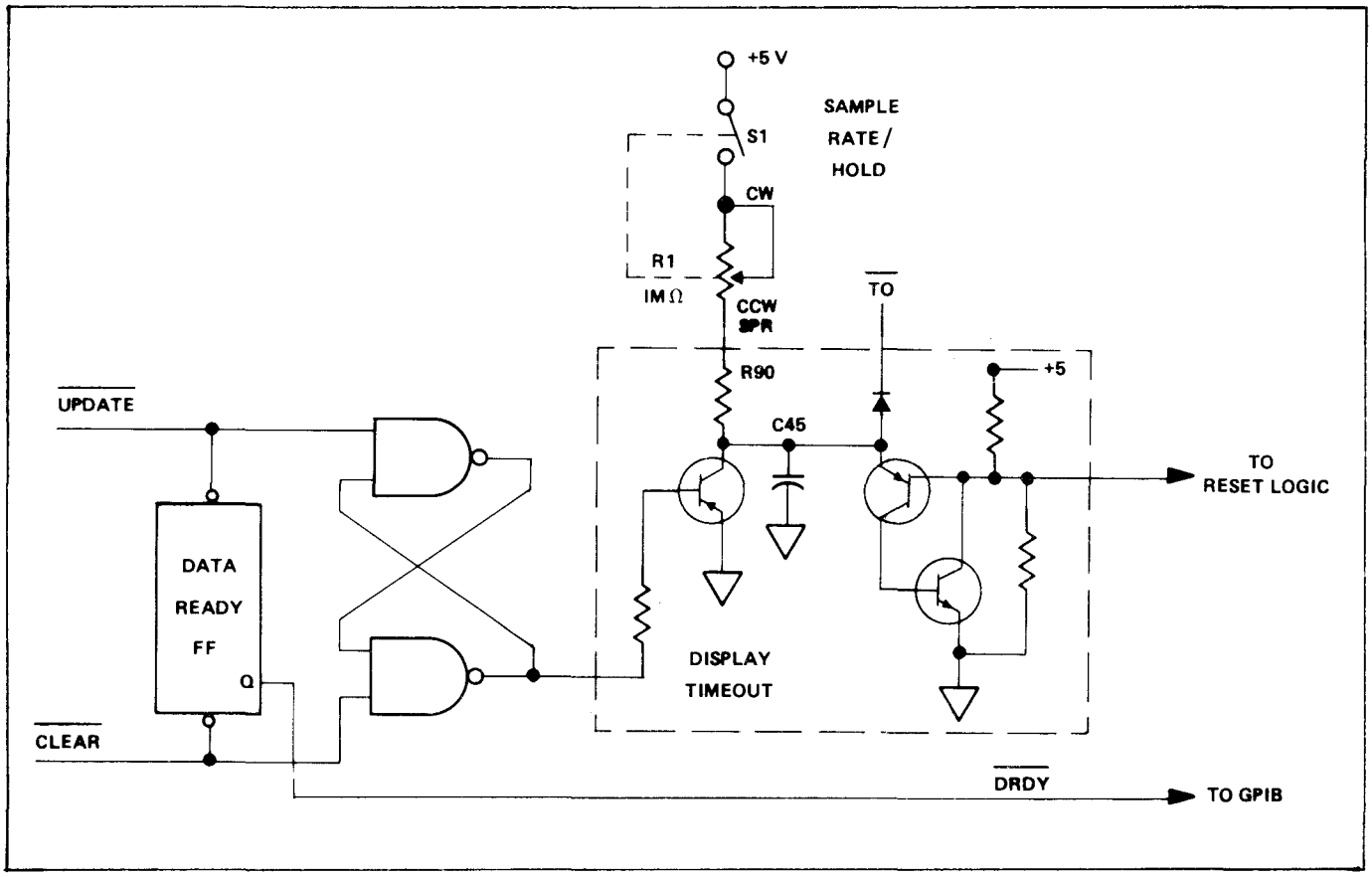


Figure 1.30 - Display Timeout Simplified Logic Diagram

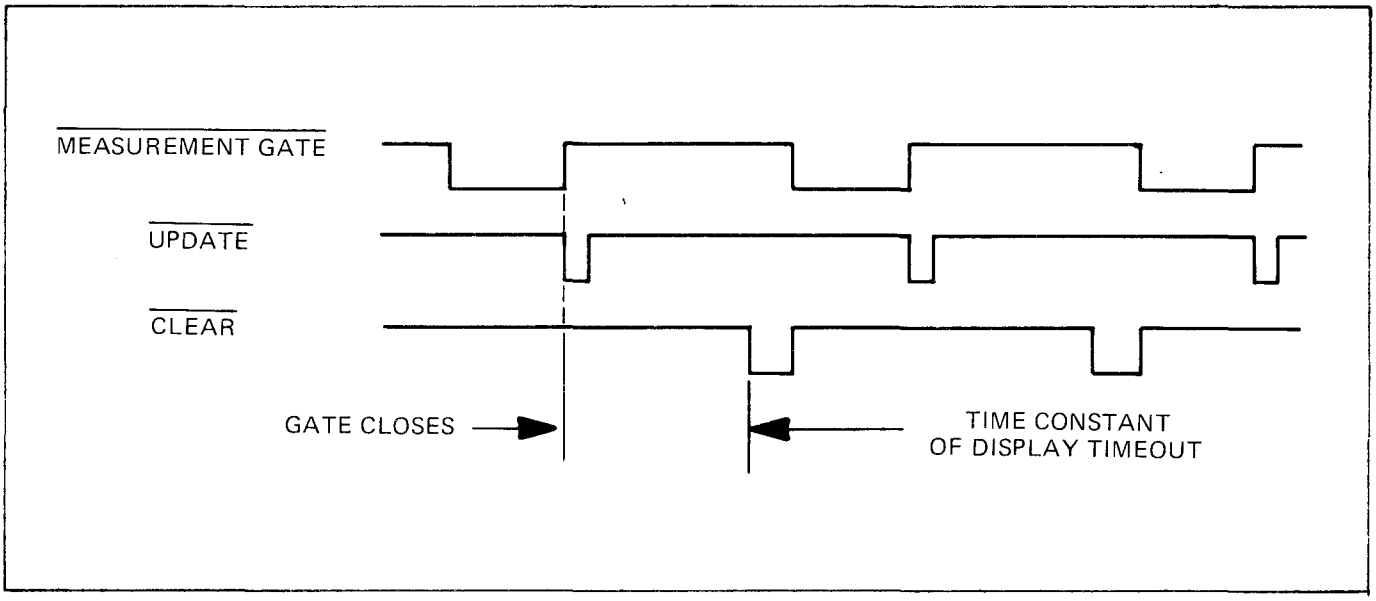


Figure 1.31 - Measurement Gate Cycle Timing Diagram

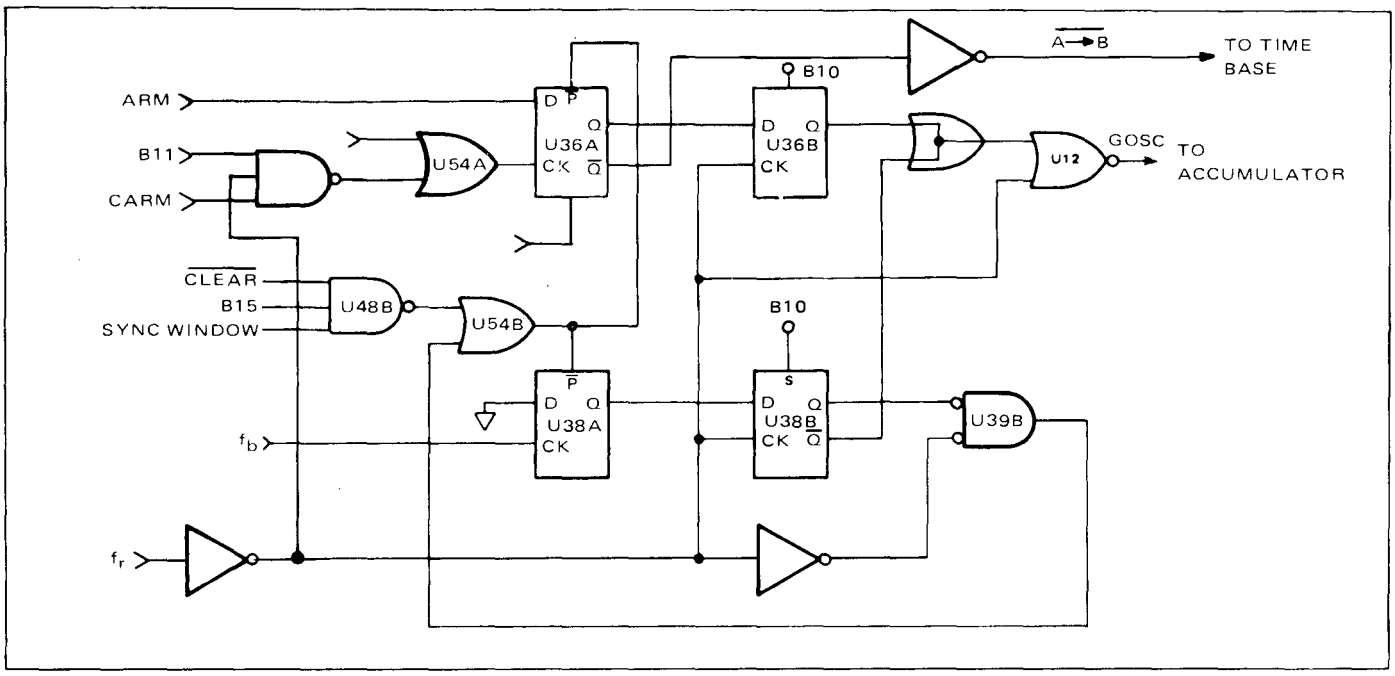


Figure 1.32 - TIA Synchronizer Simplified Logic Diagram

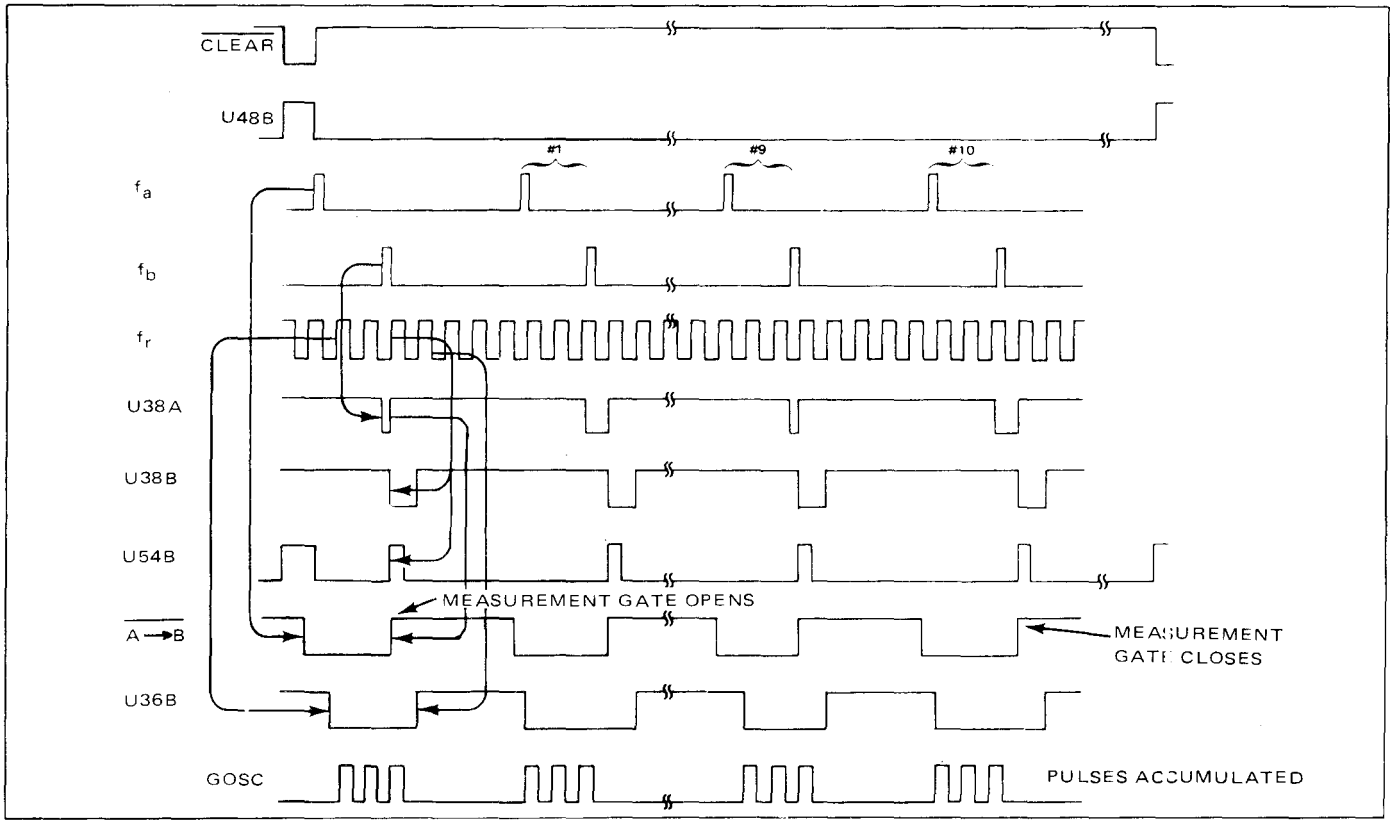


Figure 1.33 - TIA Synchronizer Timing Diagram for Averaging 10 Intervals

1.4.17.2 The $\overline{A \rightarrow B}$ signal is also used, in frequency measurement modes, to enable the first divide by ten counter U45 in the timebase circuitry and thus synchronize the start of the gate with the input signal. When the counter is armed, $\overline{ARM}$ will go low allowing U36 to be clocked low by the input signal. If the frequency mode is FA, the signal fa will cause $\overline{A \rightarrow B}$ to go low and U45 (timebase) will be enabled until the end of the gate. If the frequency mode is FC, control signal B11 will let 10 MHz through U48A to clock U36A, provided that CARM, from the RF board, indicates that there is a signal present at the FC input. In the FB mode, B12 is set high, keeping the signal $\overline{A \rightarrow B}$ low at all times and thereby allowing the gate to "free run" independently of the input signal.

1.4.17.3 In the TIA mode B10, B11 and B12 will be low while B15 will be high. After the counter is armed (ARM low), a rising edge from the start channel (fa) will clock a low level through U36A, and thus $\overline{A \rightarrow B}$ will also be set low. On the next rising edge of fr, the 10 MHz reference signal, a low level will be clocked through U36B and the oscillator clock pulses will be allowed through U39A, though they are not accumulated since the measurement gate has not opened yet. At the receipt of a stop pulse, a low level is clocked through U38A and after the next rising edge of the 10 MHz reference U38B will be clocked low. The net result will be that gate U39A will close and flip-flops U36A and U38A will be preset and after one more clock cycle U36B and U38B will also have a high logic level at their Q outputs. $\overline{A \rightarrow B}$ will have returned to a high logic level and in doing so, the measurement gate will open, allowing the accumulator to count the pulses generated by U39A during the following 10 time intervals. The steps described above will repeat for the following 10 time intervals. At the end of the tenth interval, the rising edge of $\overline{A \rightarrow B}$ will close the measurement gate and the accumulated count will be present in the accumulator.

1.4.18 Marker Out

1.4.18.1 The MARKER OUT signal on the rear panel is derived from the fa and fb signal from the signal conditioners. Signals fa and fb are translated from the ECL logic levels to TTL logic levels in differentially paired transistor circuits. See figure 1.34. The TTL signals are used to clock D-type flip-flops. The first flip-flop is clocked by fa and a high logic level is clocked through the Q-output to the second flip-flop D-input. The $\overline{Q}$-output is supplied to the rear panel MARKER OUT connector. The second flip-flop is clocked by fb and the output used to reset the first flip-flop and set the $\overline{MARKER\ OUT}$ signal high again.

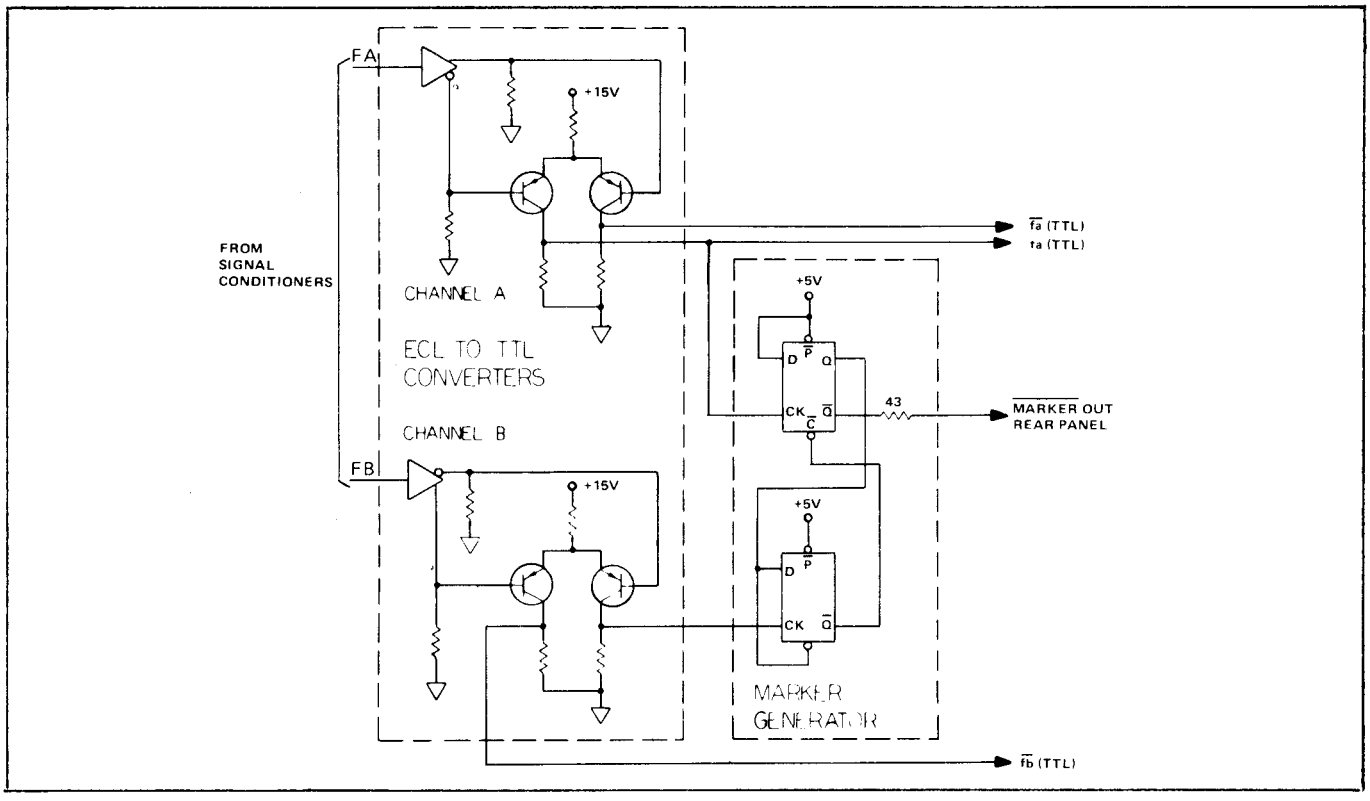


Figure 1.34 - Marker Out Simplified Diagram

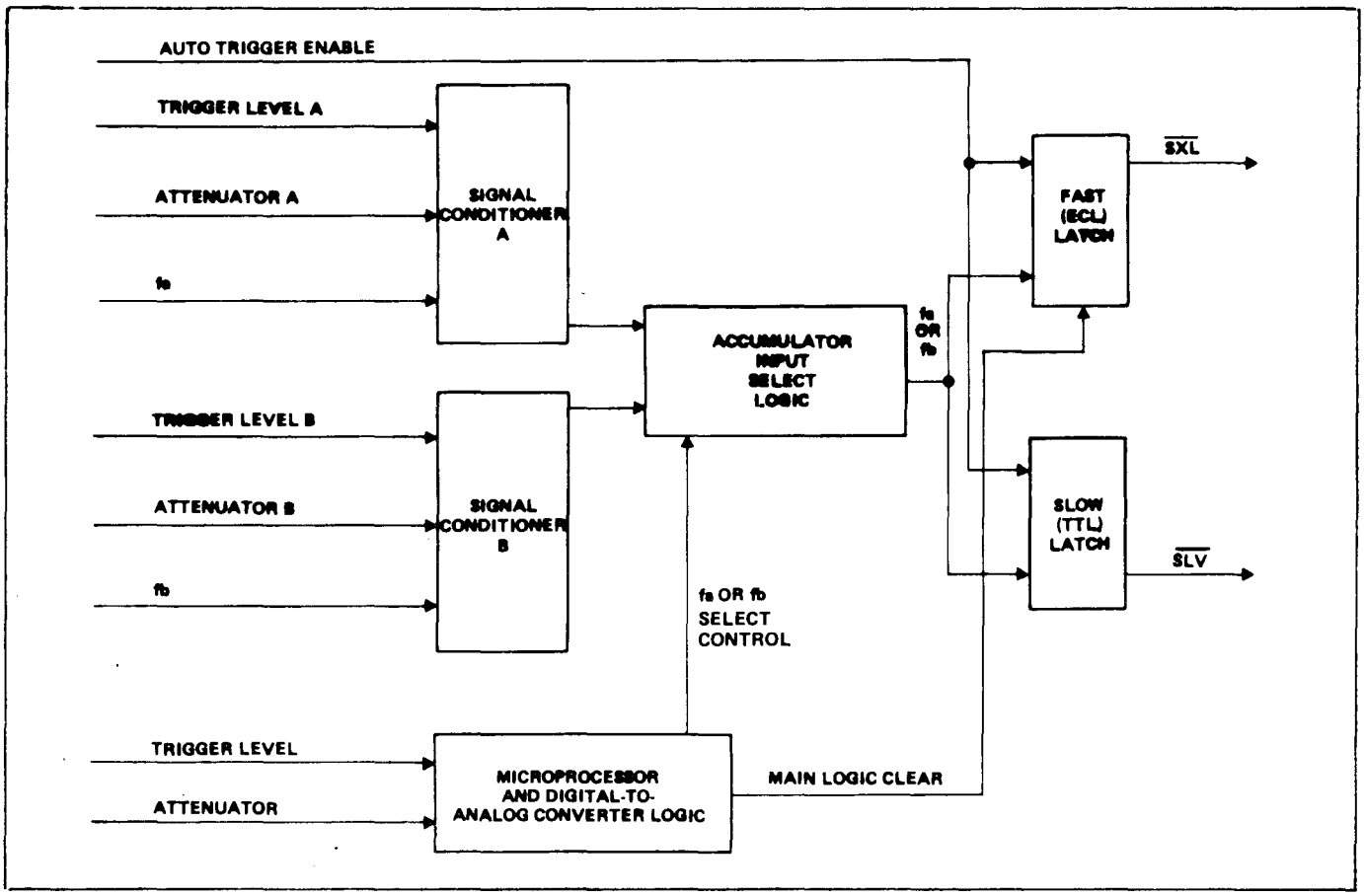


Figure 1.35 - Auto Trigger Block Diagram

1.4.19 Auto Trigger

1.4.19.1 The auto trigger circuit, in conjunction with the microprocessor and digital-to-analog logic, determines the amplitude of the incoming measurement signal and automatically sets the triggering level to an optimum point. The measurement signal is tapped at the accumulator input select logic and applied to a fast (ECL) latch and a slow (TTL) latch. See figure 1.35. The fast (ECL) latch generates a signal crossing ($\overline{SXL}$) signal if the measurement signal crosses the trigger level and the slow (TTL) latch generates a signal level ($\overline{SLV}$) signal if the measurement signal is greater than the trigger level. As shown in figure 1.36, the fast latch is comprised of NOR gate U52, flip-flop U35, and transistor Q12. The slow latch is comprised of transistor Q19 and NOR gate U47.

1.4.19.2 When the auto trigger circuit is enabled by a high level on ATE, the measurement signal of fa or fb selected by the microprocessor clocks a low level to the Q-output. Q12 turns on and a low $\overline{SXL}$ signal is sent to the microprocessor indicating that the input signal crossed the trigger level. The measurement signal is also translated to a TTL level signal through Q19, gated through U47 and sets $\overline{SLV}$ low if the measurement signal is greater than the trigger level. $\overline{SXL}$ and $\overline{SLV}$ are monitored by the microprocessor and the input attenuators and trigger level are set accordingly.

1.4.19.3 In the synchronous window mode of operation the auto trigger enable signal ATE remains low during pulses to be ignored and enables the auto trigger circuit for others. As shown in figure 1.37, only those pulses occurring when ATE is high can be seen at the signal level output.

1.4.20 512 MHz Direct Count RF Option

1.4.20.1 The 512 MHz direct count RF board automatically adjusts the amplitude of the channel C input signal to provide a suitable level for the remaining circuitry, divides the input signal frequency by ten, and generates a high, CARM logic signal when an input of the correct frequency range and of sufficient amplitude is applied to the channel C input connector. The RF board diagram, shown in figure 1.38, consists of a clipper, RF amplifier, counter, detector, and gate buffer.

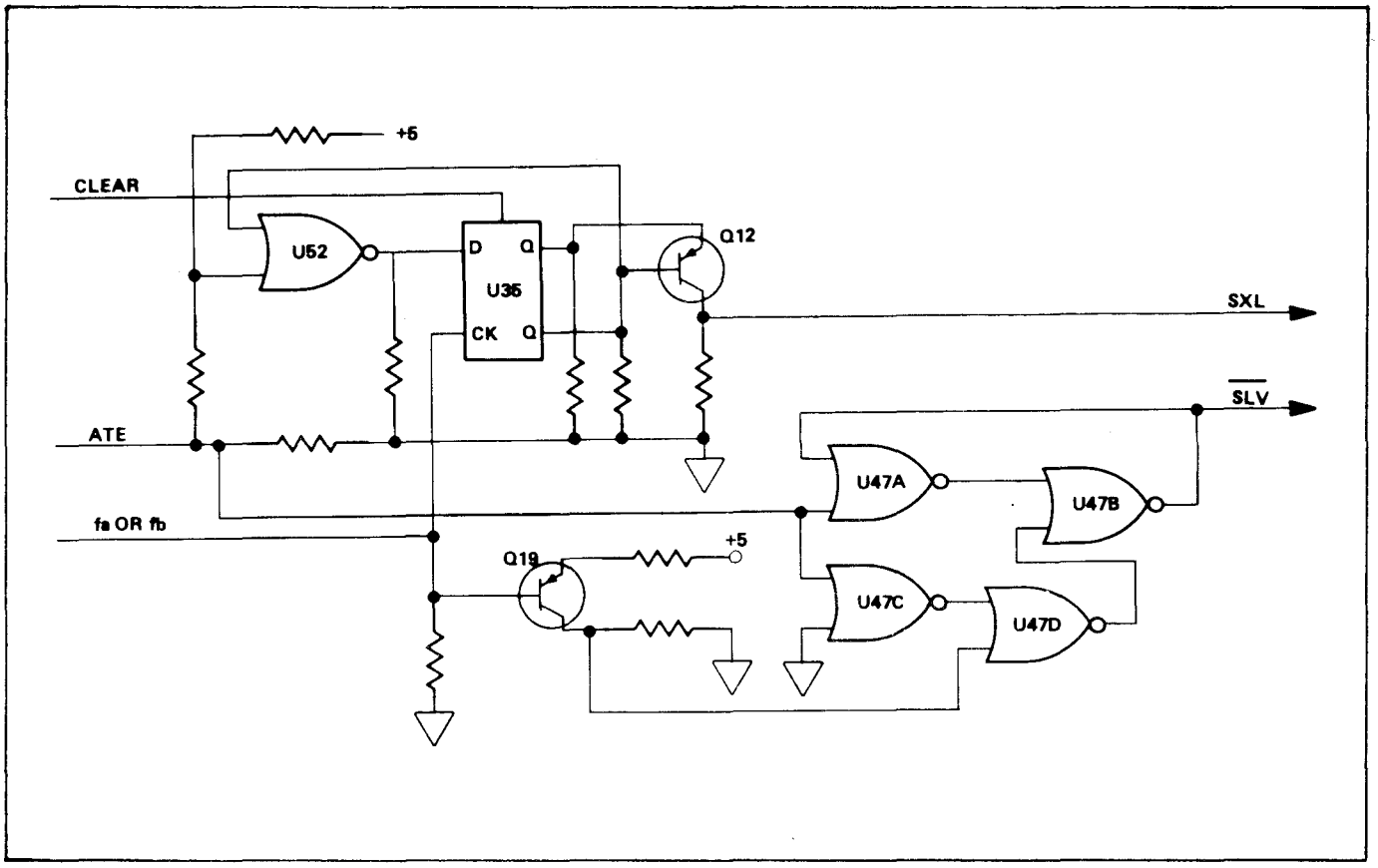


Figure 1.36 - Auto Trigger Simplified Diagram

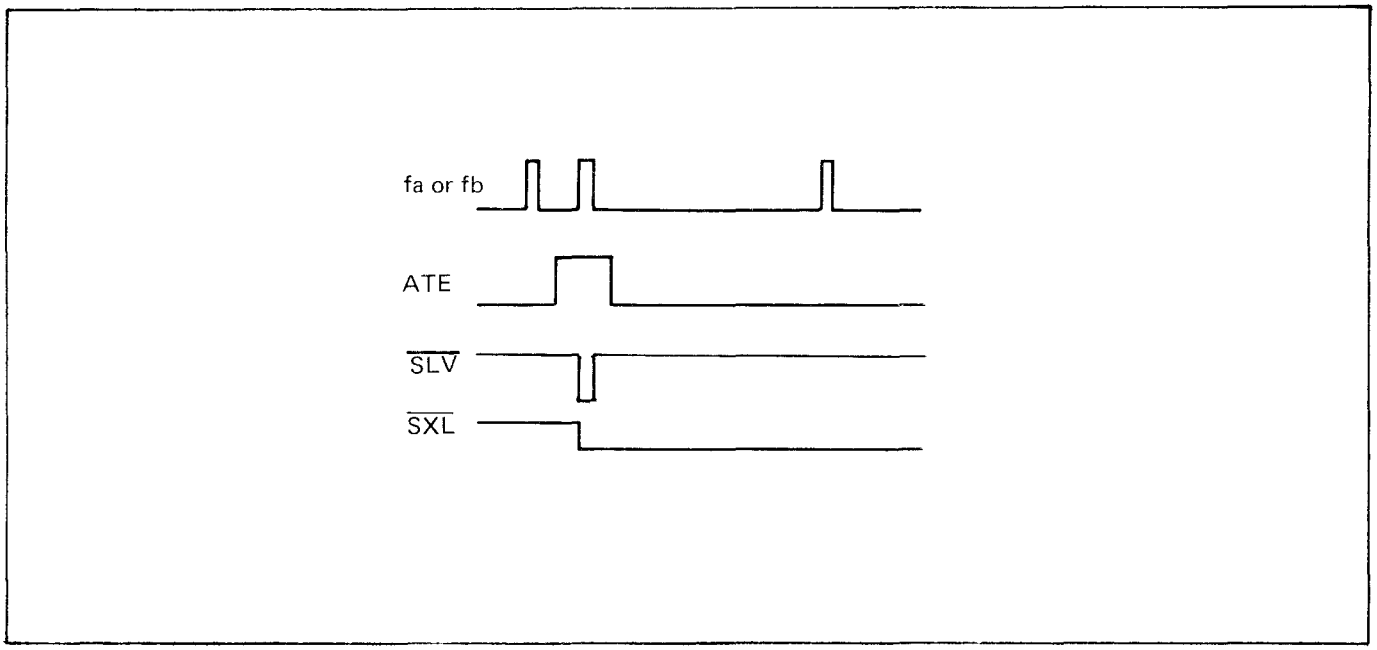


Figure 1.37 - Auto Trigger Timing Diagram

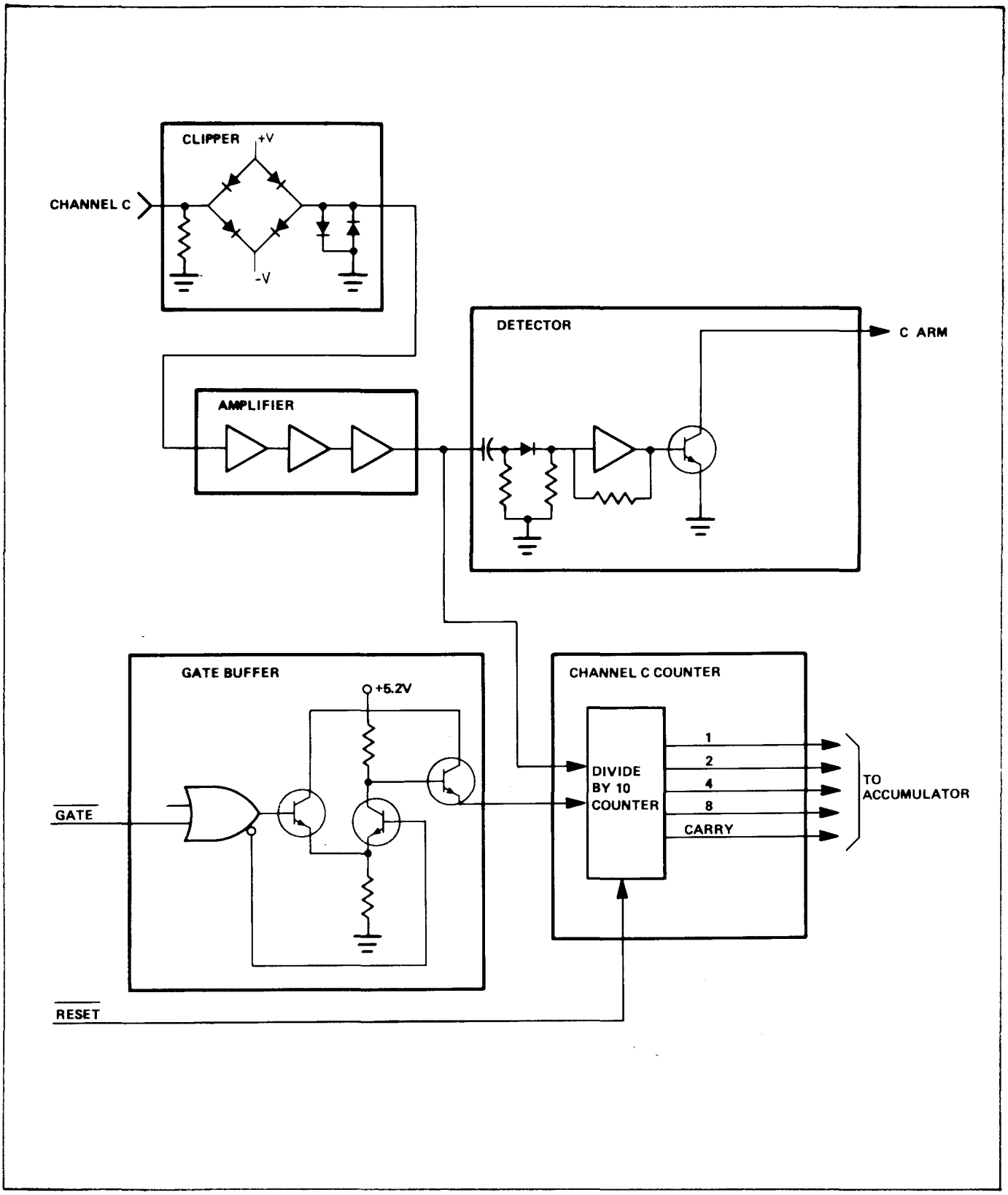


Figure 1.38 - 512 MHz RF Board Simplified Diagram

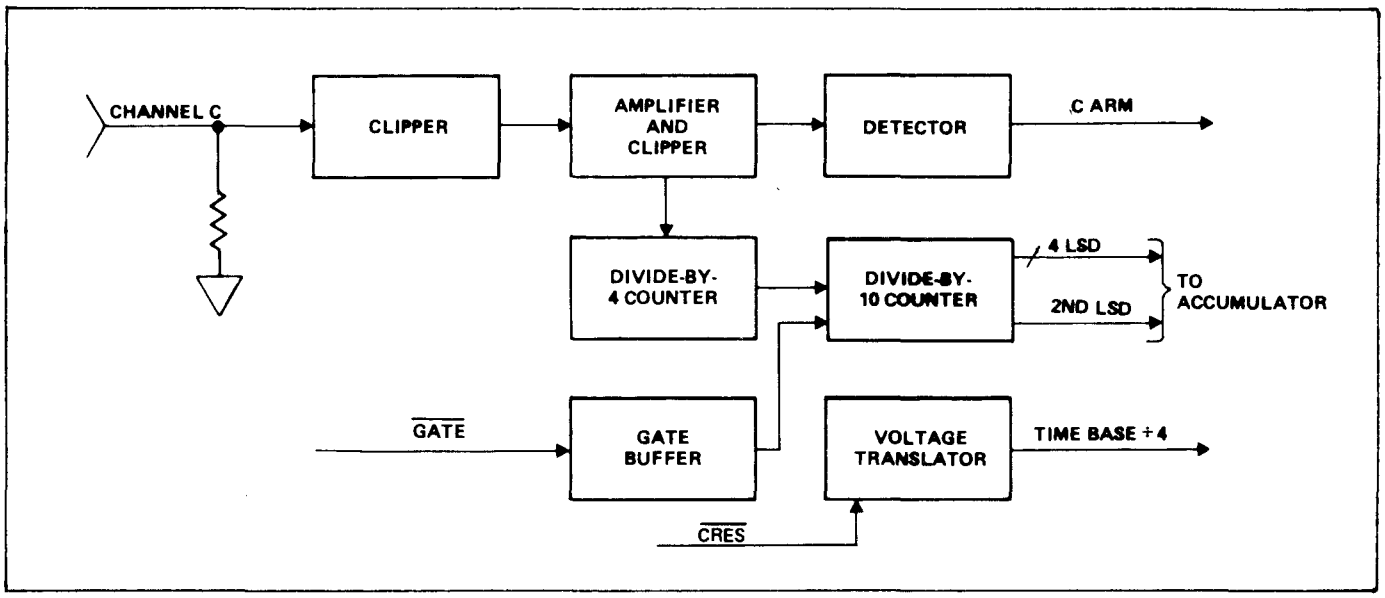


Figure 1.39 - 1.25 GHz RF Board Functional Block Diagram

1.4.20.2 The 512 MHz direct count RF board accepts signals between 50 and 512 MHz at amplitudes between 15 millivolts and 1 volt through the channel C input on the front panel. The channel C input is terminated in 50 ohms. The measurement signal is applied to a clipper circuit to limit the input to approximately 1 volt. The clipper is made up of a Schottky diode bridge in series with the signal and two diodes to shunt excess current and limit the signal to last stage of the amplifier. The amplifier circuit consists of three cascaded hybrid transistor amplifiers. The amplified output drives both the detector circuit and the channel C counter.

1.4.20.3 The detector generates the TTL logic level signal CARM indicating that the input signal to channel C is large enough to be reliably counted. The divide-by-10 counter divides the amplified signal and produces four lines of BCD data representing the least significant digit. The carry output of the counter becomes the input to the second least significant digit. The four lines of BCD data and the carry output are applied to the accumulator.

1.4.20.4 The channel C counter is a high frequency counter capable of operating past 500 MHz. The counter divides the frequency output of the amplifier by a factor of 10. The input to the counter is controlled by the GATE signal. Scaling is required to reduce the input frequency to a level compatible with the accumulator counter circuit.

1.4.21 1.25 GHz Prescaled RF Option

1.4.21.1 The 1.25 GHz prescaled RF option accepts signals up to 1.25 GHz at amplitudes between 30 millivolts and 1 volt through the channel C input on the front panel. See figure 1.39. The channel C input is terminated in 50 ohms. The measurement signal is applied to a hybrid amplifier which is internally protected against input signals up to 5 Vrms. The amplified output drives both a detector and a divide-by-four counter.

1.4.21.2 The detector generates a TTL logic level signal CARM indicating that channel C has an input signal large enough to be reliably counted. The divide-by-four and divide-by-ten counters divide the signal to frequencies compatible with the accumulator counter. The divide-by-ten counter produces four lines of BCD data representing the least significant digit. The carry output of the counter becomes the input to the second least significant digit. The four lines of BCD data and the carry output are applied to the accumulator.

1.4.21.3 An additional signal is required in the 1.25 GHz option that was not required in the 512 MHz option. A TTL level control signal is required in the timebase to enable the divide-by-four counter in that circuit to be compatible with the 1.25 GHz option board.

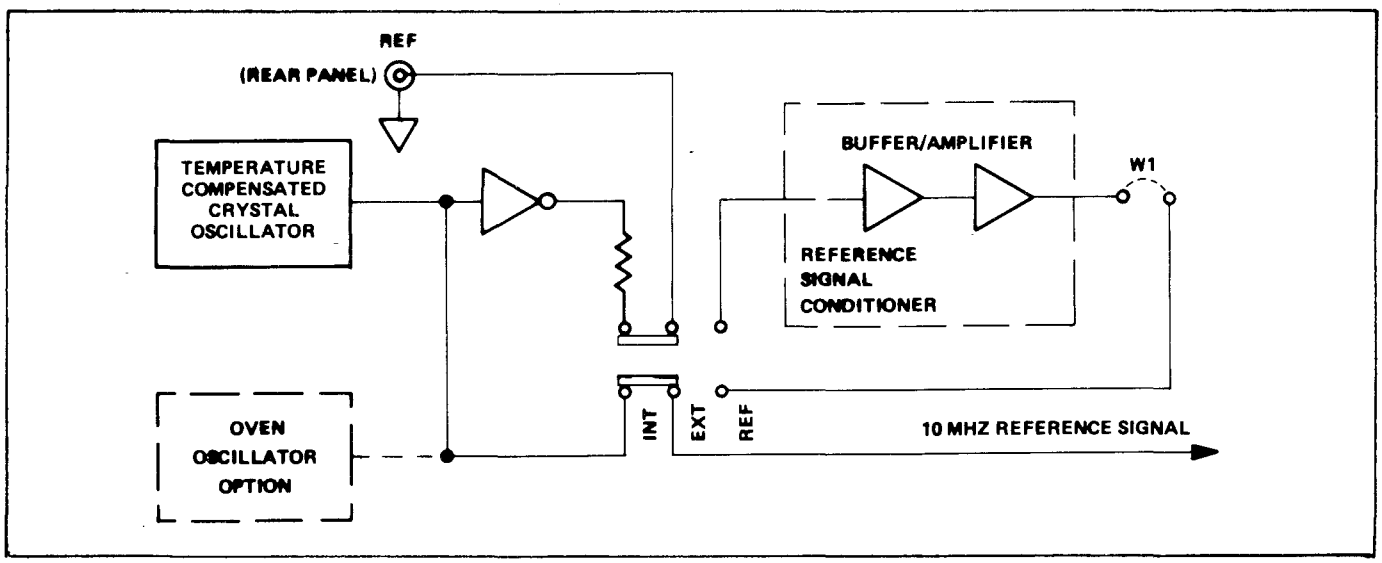


Figure 1.40 - Reference Signal Simplified Diagram

1.4.22 Reference Signal Conditioner

1.4.22.1 The 10 MHz reference signal may be supplied from three sources, the temperature compensated crystal oscillator, the optional controlled temperature oven oscillator, or an externally supplied reference signal through the rear panel REF connector. A simplified diagram of the reference signal circuitry is shown in figure 4.40. The internal reference signal may also be supplied to an external user through a buffer circuit and the REF EXT/INT switch. In the INT position the temperature controlled crystal oscillator signal or the optional oven oscillator signal are connected directly to the 10 MHz REFERENCE SIGNAL output. In the EXT position, an externally supplied reference signal applied to the rear panel REF connector is ac coupled to the reference signal conditioner through the switch. The external signal is buffered, amplified, and translated to TTL logic levels. The reference signal conditioner output is connected through jumper W1 back to the REF EXT/INT switch and to the 10 MHz REFERENCE SIGNAL output. This jumper is removed when the optional reference multiplier board is installed in the instrument.

1.4.23 Reference Multiplier

1.4.23.1 The reference multiplier board accepts a 1, 5, or 10 MHz external reference signal, filters out its 10 MHz component, amplifies it to TTL logic levels, and supplies it to the EXT REF line. See figure 1.41. Frequencies other than 1, 5, or 10 MHz are locked out. The external signal is ac coupled, and buffered in the preamplifier and used to excite a high Q resonant circuit. The resonant circuit is comprised of a 10 MHz crystal that can be shifted slightly by the external reference signal (± 10 ppm). The 10 MHz oscillator signal is buffered and amplified in the RF amplifier circuit. The output driver circuit amplifies the signal to TTL logic levels.

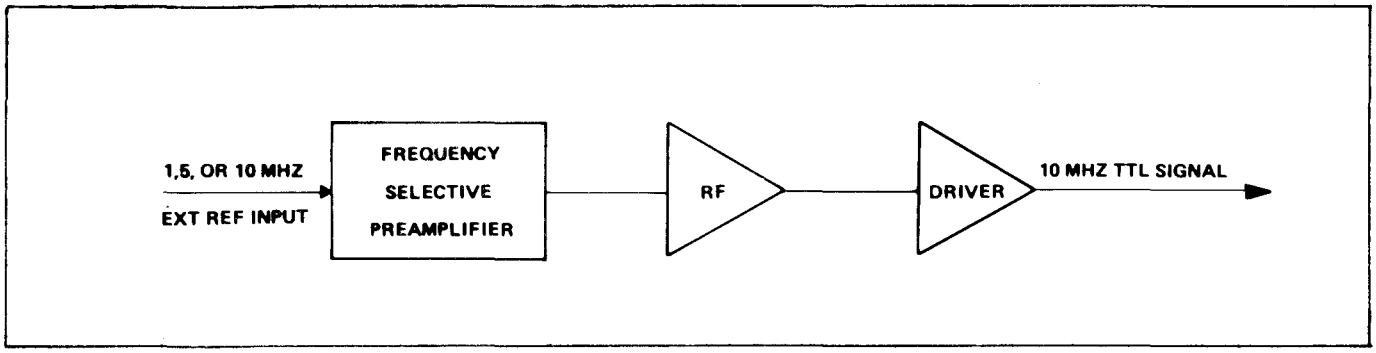


Figure 1.41 - Reference Multiplier Simplified Diagram

1.4.24 Power Supply

1.4.24.1 The power supply converts 100, 120, 220, or 240 Vac to the dc regulated power required by the TTL logic circuits, ECL logic circuits, display board, GPIB, signal conditioners, and the RF option board. The input voltage is selected by installing the jumper board in connector J14 with the supplied input voltage matching the jumper board edge installed in the connector. The fan is connected to the 120 Volt winding of the transformer and is unaffected by the input voltage selection. A simplified diagram of the power supply is shown in figure 1.42. Two rectifiers are connected to the two secondary windings of the transformer. The +5V rectifier supplies approximately 10 volts unregulated to the 7-segment LED's on the display board and to the regulator on the GPIB board. In addition, the +5V rectifier supplies the +5.2V regulator and +5V regulator. The +5.2V regulator provides power to the ECL logic circuits and signal conditioners. The +5V regulator provides power to the TTL logic circuits. The bipolar rectifier supplies a positive and a negative voltage to the +15V regulator and the −12V regulator respectively. The +15V and −12V regulators provide power to the signal conditioners, the digital-to-analog converter, and the RF option board.

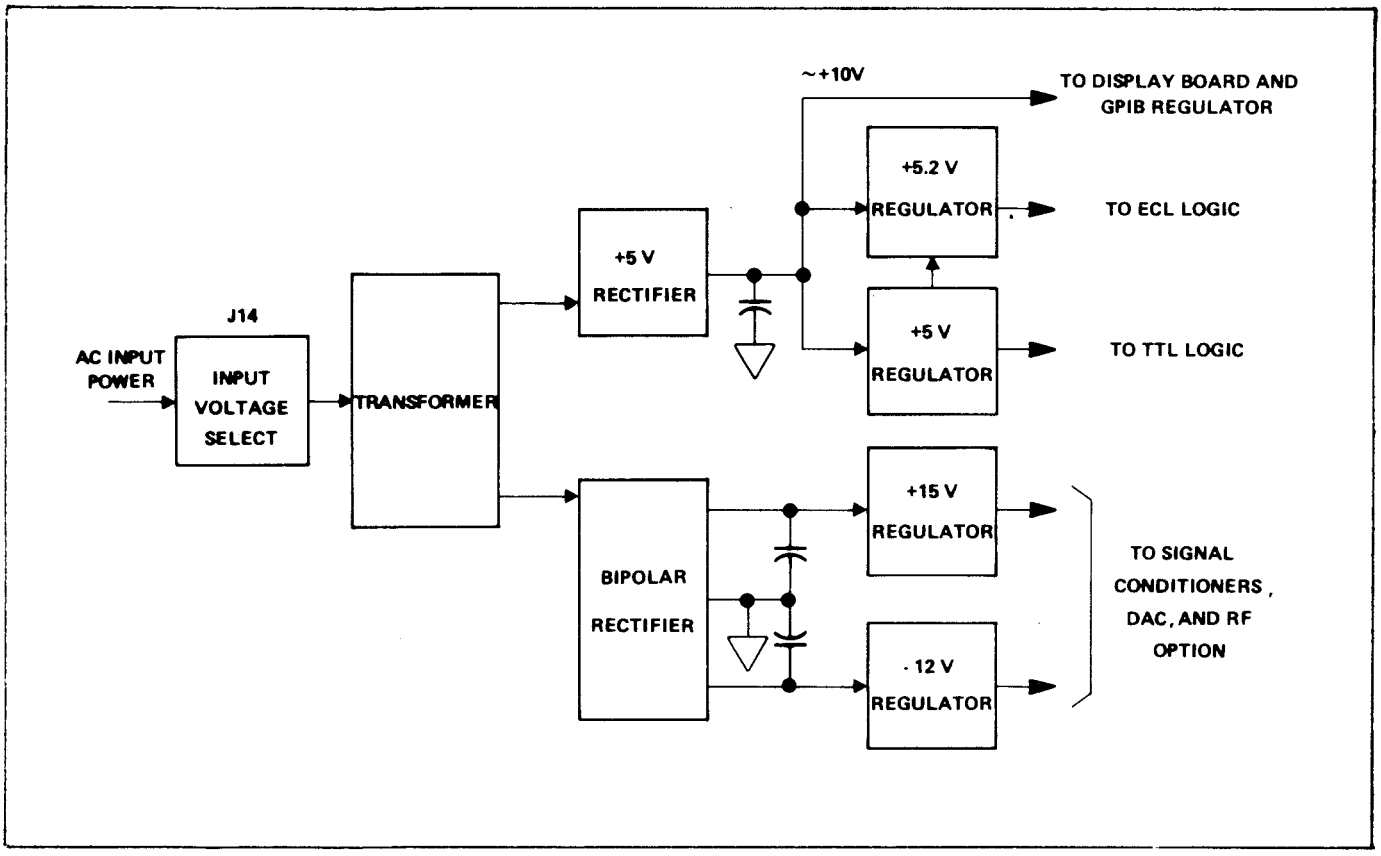


Figure 1.42 - Simplified Power Supply Diagram

1.4.25 Programming Interface (Model 9514 Only)

1.4.25.1 The 9514 Counter/Timer is configured for operation in a system through an interface compliant with the IEEE 488-1975 standard. For an introductory discussion of the above mentioned standard and how it applies to the Model 9514, see section of this manual. The Model 9514 has a different switch board from the Model 9510 and, in addition, it contains two extra board assemblies and a rotating fan on the rear panel. Physically, the two additional boards mount on a horizontal plane above the mother board and connect to it through the switch board in the front panel, and through three ribbon cables. Since signal conditioning for A and B inputs takes place on the interface assembly (GPIB board), the buffered input signals are routed to the main logic through the two coaxial cables.

1.4.25.2 A functional block diagram of the instrument is shown in figure 1.43. The diagram is divided into four major areas for the purpose of discussion; (1) Input Signal Buffers and Digital to Analog Converters (DAC), (2) Microprocessor, (3) General Purpose Interface Bus (GPIB) logic, (4) Counter Main Logic Inputs and Control.

1.4.25.3 The input signal buffers contain the input attenuators, which are selected by means of relays, circuits for implementing DC/AC coupling and 50Ω input impedance, and unity-gain low output impedance drivers. When in remote or in auto trigger mode, the trigger levels are set by a dual 9-bit binary Digital to Analog Converter (DAC). Each channel of the DAC is composed of a monolithic 8-bit DAC with an additional bit implemented in discrete circuitry.

1.4.25.4 The microprocessor used in the 9514 is an 8-bit MC6802 with 128 bytes of internal RAM. The program memory is stored in a Read-Only-Memory (ROM) and it sequences the microprocessor in a pre-determined way which accomplishes control of the instrument and operation of the interface. Communication with logic circuitry outside the processor is accomplished by decoding the address lines to produce strobe pulses which actuate latches if an output operation is to be performed or tri-state input switches if in the case of input operations.

1.4.25.5 The GPIB logic consists of bi-directional buffers for the IEEE 488-1975 Bus, tri-state drivers to input information to the processor and latches to output information onto the bus.

1.4.25.6 The Counter Main Logic inputs and control is composed of tri-state input switches and latches (for I/O operations from the processor). Control of the main logic board is accomplished via the output latches. The status of the counter is transmitted to the processor through the tri-state input switches.

1.5 PROGRAMMING INTERFACE DETAILED CIRCUIT DESCRIPTION

1.5.1 Input Signal Buffers and DAC

1.5.1.1 Refer to the schematic IEEE 488-1975 Interface, sheets 4 and 5, on pages and for the following discussion. The input buffers consist of coupling and attenuation circuitry switched by relays and two-stage unity gain buffers. Table lists the control signals for the input and their effect on the relays. The unity gain buffers consist of a FET in the common drain configuration followed by a bipolar transistor in the common collector configuration, forming an low-output-impedance driver. In order to compensate for offset voltages and drift, identical paths are followed by the input signal and the trigger level of each input channel. Protection to the input FET is provided by diode clamp circuitry. Assume that the input signal to channel A is much greater than the allowed over-range of 300%. Diode CR19 at the gate of Q8A will conduct, effectively clamping the voltage at this point to the voltage of zener diode CR13 (3.3V). In the case of large negative voltages diode CR2 will accomplish the same clamping function. Current through the diodes is limited by resistors R28 and R29. The diode clamp of channel B operates the same as channel A. Selection of trigger level source is accomplished through U13, an analog FET switch. Whenever the instrument is in remote operation or if the auto-trigger mode is selected, the trigger levels will be taken from the output of the digital to analog converter; otherwise, the trigger levels are derived from the front panel trigger level potentiometers.

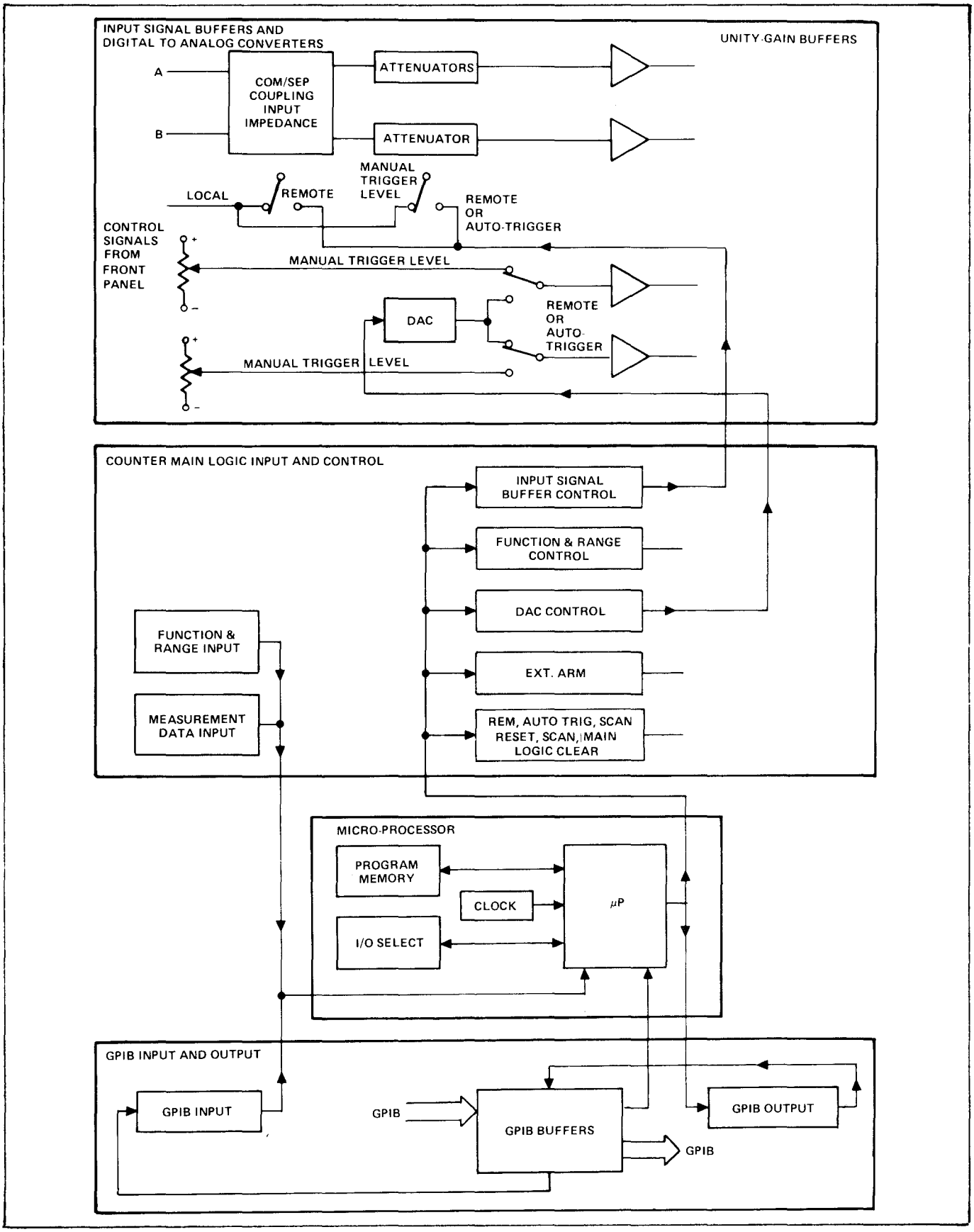


Figure 1.43 - Functional Block Diagram

1.5.1.2 Figure 1.43 shows the schematic of the digital to analog converters for the Model 9514 counter. Each channel contains a 9-bit shift register which receives binary coded information in a bit-serial format (LSB first) and transforms it into a 9-bit parallel word that defines the trigger level for that channel. The LSB of the DAC is equal to a 12.5 mV increment. Table 1.10 shows the range of the DAC and its binary limits.

Table 1.10 - Binary Coding of DAC Output
(Voltage Resolution is 12.5 mV)

Binary Word	DAC Level
0 0000 0001	-3.1875 volts
1 0000 0000	0.00 volts
1 1111 1111	+3.1875 volts

1.5.1.3 The 9 bit DAC is composed of a monolithic 8-bit digital-to-analog converter (DAC) and a current source which forms the 9th bit (MSB) stage. Integrated circuit U10 acts as a current sink controlled by its binary input from U9. When the binary input equals zero, no current is sunk by U10. Conversely, when the input word is all ones, a current of approximately 2 mA is drawn by U10-4. Flip-flop U8, one transistor of U11 and Q6 form the most significant bit of the digital to analog converter. When U8-9 is low, current source Q6 is turned on, providing approximately 2 mA of current. This current splits in two parts. One portion enters pin 4 of U10, its magnitude being controlled by the binary word present in U9, and the rest is transformed into a voltage by a transimpedance amplifier formed by U7 and Q5. The gain of this amplifier is equal to the negative of the value of R23. The DAC for channel B trigger level works in a similar manner to channel A.

1.5.1.4 A stable reference for both channels is provided by utilizing one of the transistors in array U11 with its emitter-base junction reversed biased into a breakdown mode. Temperature compensation is accomplished by placing two forward biased base-emitter junctions in series. Unity gain amplifier U7 acts as a buffer and its output serves as a voltage reference for U10, U3, Q6 and Q3. The bases of current source transistors Q3 and Q6 are fixed to a voltage derived from the reference voltage by the unity-gain amplifier comprising Q2 and Q4.

1.5.2 Microprocessor

1.5.2.1 Figure 1.44 shows a simplified block diagram of the microprocessor section and associated circuitry. Upon the application of power, the microprocessor's reset input remains low for the time that it takes capacitor C70 to charge up to the threshold of the reset input. At that time, the microprocessor receives program information from U22 and executes a predetermined sequence of steps. The clock for the microprocessor (μP) is derived from the instrument's 10 MHz reference through a divide-by-three circuit. The clock for the display scan circuitry (U9 on main logic board) derives its clock by dividing the enable output of the μP by 32, and thus synchronizing the scan frequency of the display to the execution cycle of the μP.

1.5.2.2 The requirements of the IEEE 488-1975 are such two of the control lines of the interface bus, IFC and REN, must produce a response from the instrument within 100 μsec. In order to meet this requirement, these two lines are brought to the interrupt inputs of the μP. Whenever IFC is asserted or the processor interrupts whatever sequence it is executing and proceeds to clear the interface within 100 microseconds. If REN was deasserted the instrument goes into local mode within 100 microseconds.

1.5.2.3 The processor transmits and receives data by sending control signals via the I/O strobe generator. To acquire input data the processor sends data strobes to tri-state switches which momentarily connect the processor bus to either the counter main logic or to the GPIB bus. To transmit information to the counter main logic or over the GPIB bus, the processor transmits signals via the I/O Strobe generator to latches which in turn apply the processor output data to the GPIB or counter logic.

1.5.3 Main Logic Input and Control

1.5.3.1 The Main Logic Input and Control circuitry will be partitioned into three sections for the purposes of the following discussion; (1) Status and Measurement Data Input, (2) Main Logic Control Circuitry, and (3) Auto Trigger Logic.

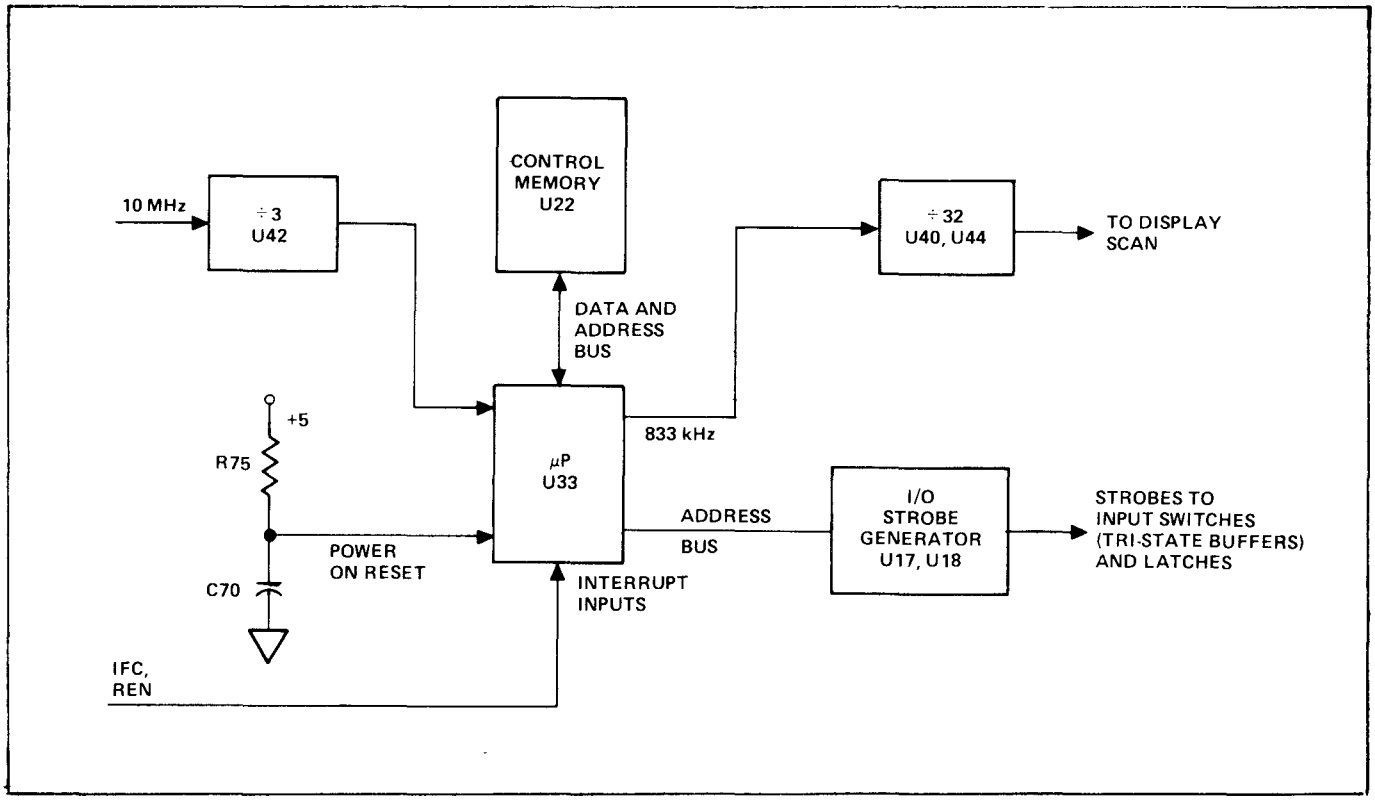


Figure 1.44 - Microprocessor Simplified Block Diagram

1.5.3.2 STATUS AND MEASUREMENT DATA INPUT

1.5.3.2.1 Figure 1.45 shows a simplified schematic of the Status and Measurement Data Input switches. The processor receives the status of the instrument by sending a strobe signal to the input tri-state switches. Upon receipt of the strobe, the FUNCTION AND RANGE coded information is placed on the processor data bus. Table 1.11 shows the binary code corresponding to each function and range.

1.5.3.2.2 To receive measurement data, the processor monitors the $\overline{\text{DATA READY}}$ line. Whenever this line goes low, it indicates that the accumulator contains valid measurement data. The data is presented to the μP with the first eight least significant digits time-multiplexed on lines STA through STD, the ninth digit on lines D9A through D9D and the overflow signal on the line labeled OFF.

1.5.3.2.3 In order to de-multiplex the first eight digits, a pulse is sent to the multiplexing circuit (SCNR signal) which causes the display scan to start at the 8th most significant digit. At the same time, the signal SCNR clears U40, which provides the clock for the display multiplexers, ensuring that a new data digit will be presented to the μP every 38 μsec. The control program for the processor causes each digit to be read at the proper time. The ninth digit code and the overflow signals are simply transmitted to the processor without the above timing considerations since they are valid whenever $\overline{\text{DATA READY}}$ is low.

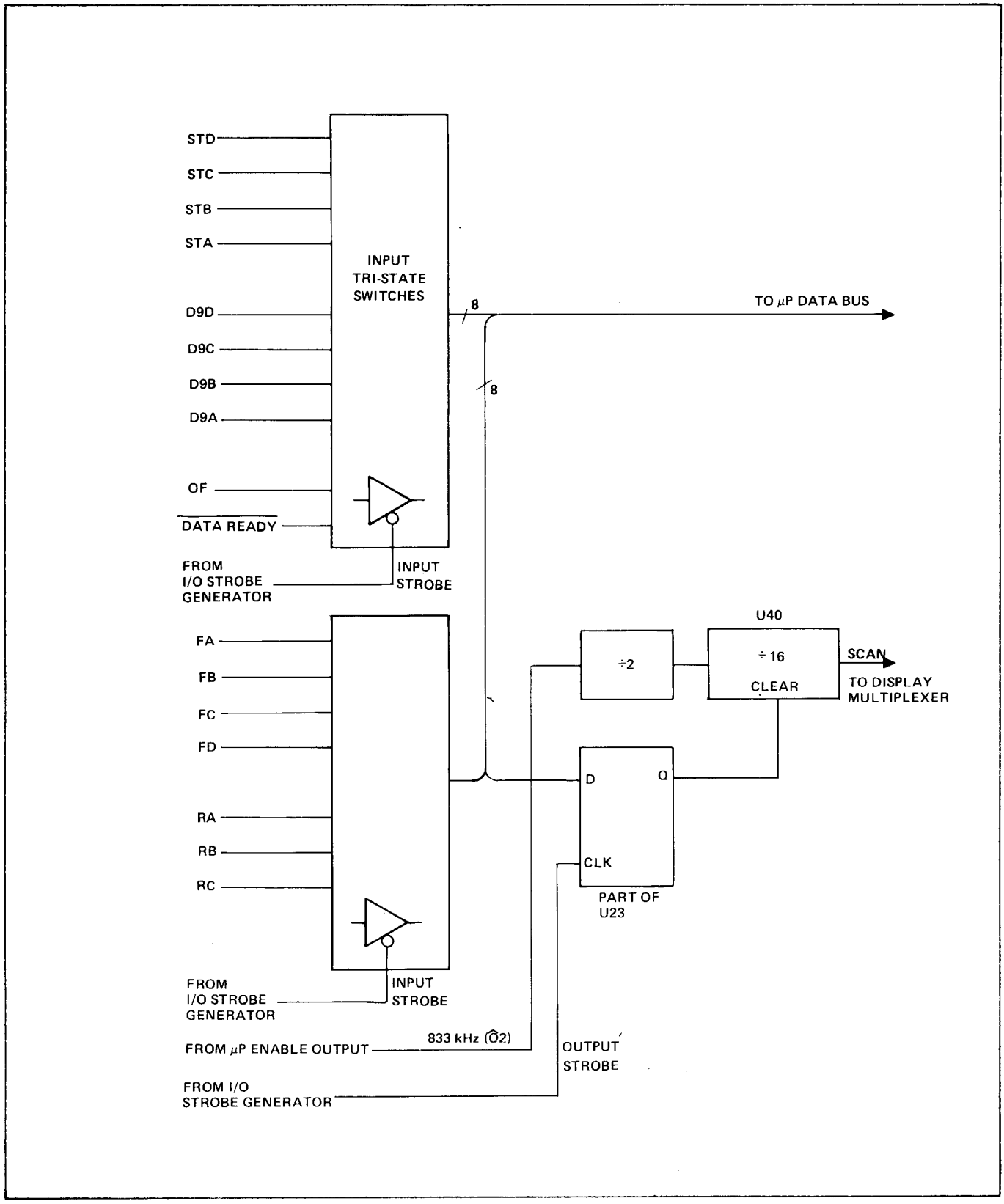


Figure 1.45 - Status and Measurement Data Input Simplified Schematic Diagram

Table 1.11 - Function and Range Coding

Function	Code				N/RESOL	Code		
	FD	FC	FB	FA		RC	RB	RA
FA	0	0	0	0	0/1 MHz	0	0	0
FC	0	0	0	1	1/0.1 MHz	0	0	1
R B/A	0	0	1	0	2/10 kHz	0	1	0
R C/A	0	0	1	1	3/1 kHz	0	1	1
P	0	1	0	0	4/0.1 kHz	1	0	0
TI	0	1	0	1	5/10 Hz	1	0	1
PA	0	1	1	0	6/1 Hz	1	1	0
TIA	0	1	1	1	7/0.1 Hz	1	1	1
FB	1	0	0	0				
C/A→B	1	0	0	1				
TOT	1	0	1	0				
AUT A	1	1	1	0	} Used during auto-trigger search only.			
AUT B	1	1	1	1				

1.5.3.3 MAIN LOGIC CONTROL CIRCUITRY

1.5.3.3.1 Figure 1.46 shows a simplified diagram of the Main Logic Control Circuitry. Function, resolution and external arming mode are programmed by the processor by shifting the control signals into a nine-bit shift register under control of the I/O strobe generator. Notice that actual control of these lines does not take place if $\overline{\text{RMT}}$ is in a high state, since the tri-state drivers will be disabled. $\overline{\text{RMT}}$ will be set low by the processor when commanded to go into remote by the controller or if an auto trigger command is detected from the front panel switches.

1.5.3.3.2 The input signal conditioners and attenuators are programmed by the processor through a second 9-bit shift register under control of the I/O strobe generator. Full control of the input signal conditioners and attenuators takes place when the external controller commands the instrument into its remote mode. At this point in time, both $\overline{\text{RMT}}$ and CNF will go to a low level and the tri-state drivers will be enabled.

1.5.3.3.3 In the auto trigger mode, it is desired that coupling, slope and input configuration be controlled by the front panel. In this case, CNF will remain high, and the signal AUTA or AUTB will cause the attenuator and trigger level to be controlled by the processor. The trigger level multiplexer inputs are the front panel potentiometers and the DAC, and it selects one of these sources as the trigger level control. When the instrument is in remote or auto trigger mode the DAC controls the trigger level; otherwise the front panel potentiometer is selected.

1.5.3.3.3 A hex latch is used for programming of gating modes. CNF controls the tri-state drivers for the input signal conditioners. The signal UPDR causes the accumulator's contents to be latched and displayed. Under certain conditions the external controller may desire a partial accumulation of counts during a measurement. Since the processor obtains the measurement data from the display latches, the need arises to be able to transfer the accumulator's count into the display even though the measurement may not have ended. A negative going pulse on UPDR will cause this transfer. To clear the counter, the processor issues a negative going pulse MLCL through a one-shot multivibrator.

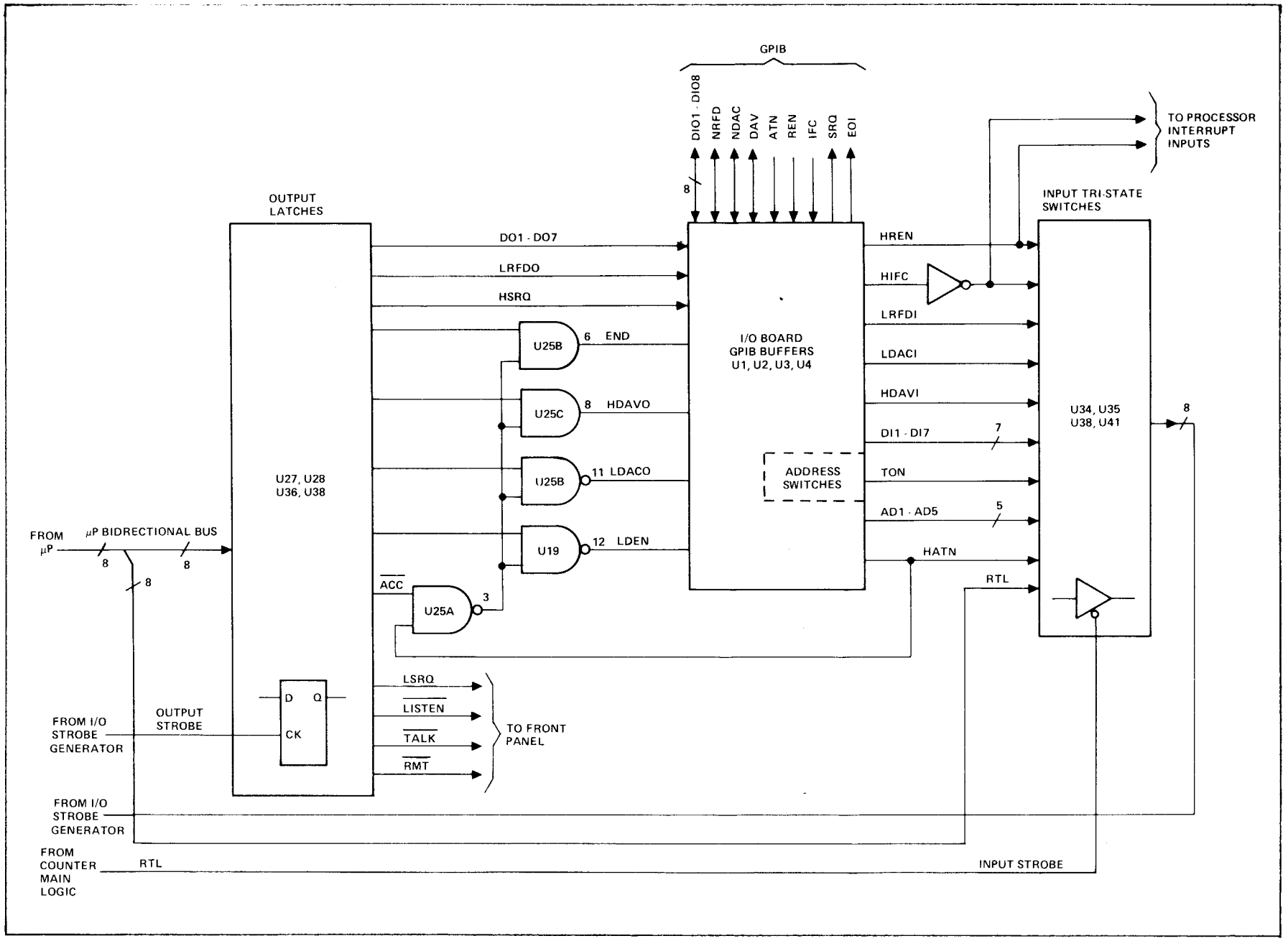


Figure 1.46 - Main Logic Control Circuitry Simplified Diagram

Table 1.12 - Main Logic Control Signals

<table>
<tr><th>Mnemonic</th><th>Description</th></tr>
<tr><td>AUTA</td><td>Signal from front panel switchboard. When low it indicates that user has switched channel A attenuator switch into its auto position, disabling front panel control of attenuator relays and trigger level. Processor controls attenuator and trigger level by means of A1A and A2A and DAC.</td></tr>
<tr><td>AUTB</td><td>Same as above for channel B. A1B and A2B control attenuator.</td></tr>
<tr><td>$\overline{\text{RMT}}$</td><td>Low when unit is in remote or if it is executing a peak search (auto trigger).</td></tr>
<tr><td>CNF</td><td>If instrument is in remote, signal will be low allowing processor control of coupling, slope and input configuration (COM/SEP/TEST). If an auto trigger peak search is in progress, or if unit is in local, this signal will remain high.</td></tr>
<tr><td>SWDC</td><td>Inverted version of CNF. When high it disables front panel switches SEP/COM/TEST and +/–, DC/AC for both channels.</td></tr>
<tr><td>FA through FD</td><td>Function program lines. See Table 1.11 - Function and Range Coding.</td></tr>
<tr><td>RA through RC</td><td>Resolution program lines. See Table 1.11 - Function and Range Coding.</td></tr>
<tr><td>$\overline{\text{TEST}}$</td><td>When low, the input signal conditioners are disabled and the 10 MHz reference is applied to the counter circuitry.</td></tr>
<tr><td>$\overline{\text{DCA}}$, $\overline{\text{DCB}}$</td><td>DC coupling control signal for channels A and B respectively. When low, DC coupling is commanded.</td></tr>
<tr><td>$\overline{\text{PSA}}$, $\overline{\text{PSB}}$</td><td>Active low positive slope control signal for channels A and B respectively.</td></tr>
<tr><td>A1A
A2A</td><td>Attenuator control for channel A.
<table>
<tr><th>A1A</th><th>A2A</th><th>Range</th></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>10</td></tr>
<tr><td>0</td><td>1</td><td>100</td></tr>
</table></td></tr>
<tr><td>A1B
A2B</td><td>Attenuator control for channel B.
<table>
<tr><th>A1B</th><th>A2B</th><th>Range</th></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>10</td></tr>
<tr><td>0</td><td>1</td><td>100</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{MLCL}}$</td><td>Low going pulse approximately 150 μsec long. It clears all measurement logic and the $\overline{\text{DATA READY}}$ signal. Unless external arming is used, it arms counter for new measurement.</td></tr>
</table>

Table 1.12 - Main Logic Control Signals continued

Mnemonic	Description
GDR	Gate delay control. When in remote, a low level on this line programs the gate delay mode. This line is always high when counter is under local control.
SWR	Synchronous window control. When in remote, a low level on this line programs the synchronous window mode. This line is always high when counter is under local control.
EAER	External arm control. When in remote, a low level on this line programs the external arming mode. This line is always high when counter is under local control.
UPDR	Display latch update control. A low going pulse on this line causes the display to latch whatever measurement is present on the accumulator. It is used to transmit to the controller readings "on the fly".

1.5.3.4 AUTO TRIGGER LOGIC

1.5.3.4.1 Refer to figure 1.47 for the following discussion. Whenever the front panel range switches for channels A and B are set to the auto trigger mode position the signals AUTA and AUTB will be low respectively. If the auto trigger pushbutton for channel A is pressed, the de-bounce flip-flops will send a signal to the input hi-state switches. The processor detects auto trigger commands by periodically enabling the tri-state switches. If a switch closure is detected, the processor will bring $\overline{\text{RMT}}$ low while leaving CNF high and send the function code corresponding to Auto Trigger channel A or B to the main logic board.

1.5.3.4.2 The peaks of the input signal are detected by a successive approximation technique. The lines $\overline{\text{SXL}}$ and $\overline{\text{SLVL}}$ give an indication to the processor of the position of the trigger level with respect to the input signal. If the trigger level crosses the input signal $\overline{\text{SXL}}$ will go to a low level. In the event that the input signal does not cross the trigger level, $\overline{\text{SLVL}}$ in conjunction with knowledge of the programmed slope for the channel under consideration will indicate to the processor whether the trigger level is more positive or negative than the peaks or valley of the input signal.

1.5.3.4.3 The processor must wait at least one full period of the input signal before it can assume that the trigger level will not be crossed by the input waveform. Since the frequency of input signal can be near zero, a time limit must be set. A one-shot multivibrator is used for this purpose. Each time the trigger level is set, the one-shot flip flop is started, and the processor waits until the multivibrator times out to read $\overline{\text{SXL}}$ and $\overline{\text{SVLV}}$. The state of these lines is used to generate a new trigger level, and $\overline{\text{SXL}}$ is cleared by $\overline{\text{MLCL}}$ to start a new cycle. This process is continued until the desired peak is found. Once $\overline{\text{SXL}}$ goes low indicating a signal crossing it is not necessary to wait any longer, so $\overline{\text{SXL}}$ is brought to the clear input of the one-shot multivibrator, causing to time-out.

1.5.3.4.4 The use of an external device allows the use of the same software module for different wait times. The Model 9514 auto trigger algorithm is specified to work with signals down to a frequency of 400 Hz. If a lower operating frequency is desired, the timing elements of the one-shot multivibrator may be changed accordingly.

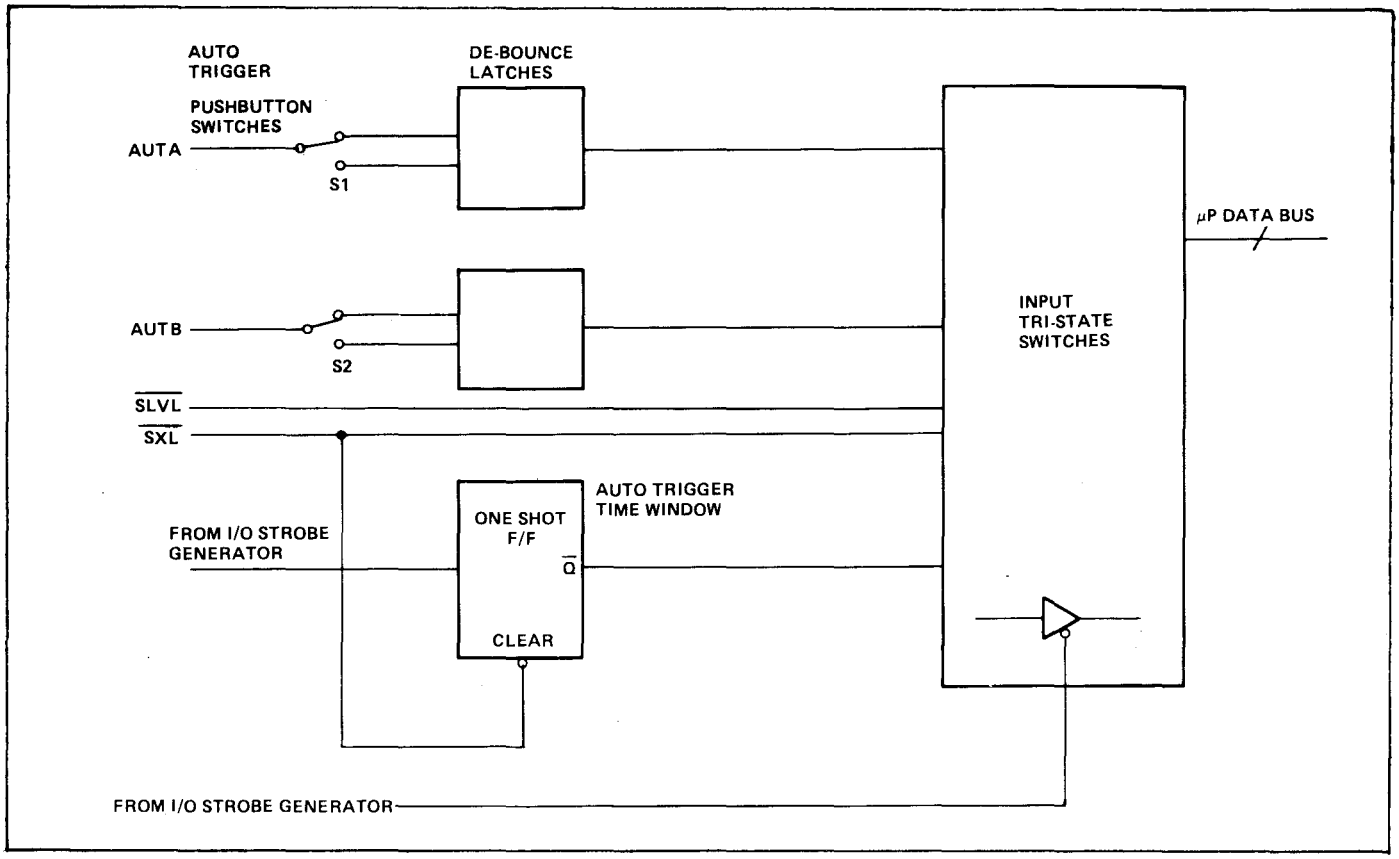


Figure 1.47 - Auto Trigger Logic

Table 1.13 - Auto Trigger Logic Signals

Mnemonic	Description
AUTA AUTB	Signals from front panel switches. A low on these signals indicates that the auto trigger mode is selected for channel A or B respectively.
$\overline{SXL}$	Latched signal from main logic board. A low indicates that the trigger level set by the DAC has been crossed at least once by the input waveform. $\overline{SXL}$ is cleared by the processor by issuing a negative pulse on $\overline{MLCL}$.
$\overline{SLVL}$	Signal from the output of the input comparator. The following table describes the conditions that affect $\overline{SLVL}$.

Condition of Trigger Level	Slope	$\overline{SLVL}$
Trigger level > Peak of Input Signal	+	0
	-	1
Trigger level < Valley of Input Signal	+	1
	-	0

1.5.4 General Purpose Interface Bus Logic

1.5.4.1 The GPIB logic is illustrated in 1.48. As shown in the illustration this logic comprises the output latches, the input/output board GPIB buffers and the input tri-state switches. The output latches control the flow of information between the microprocessor by directional bus and the I/O board. In addition the output latches provide the drive signals for the front panel GPIB status annunciators. The following discussion assumes that the reader is familiar with the IEEE488-1975 standard. For a simplified description of the interface standard refer to the operator's manual.

1.5.4.2 As previously discussed the microprocessor transmits data by generating an output strobe which causes the latches to set to the information contained on the microprocessor data bus. To read information in from the GPIB via the I/O board and GPIB buffers the microprocessor sends an input strobe to the tri-state switches and the information from the I/O board is applied to the bi-directional microprocessor data bus. Table 1.15 lists GPIB logic signals.

1.5.4.3 The I/O board includes the address selection switches used for assigning the counter a GPIB address. The TALK ONLY mode is also selected by means of a switch on the I/O board. Instructions for assignment of bus address are included in the Model 9500 Operating Manual.

Table 1.14 - Status of Handshake Control Lines in the Idle Mode

Control Line	State
HDAVO	Low
LDACO	Low
LRFDO	Low
END	Low
$\overline{ACC}$	High
LDEN	High

1.5.4.4 OPERATING MODES

1.5.4.4.1 As a bus member the Model 9514 has 3 basic operating modes. These are (1) acceptor, (2) source and (3) idle. The instrument initializes into the idle mode when power is applied. In this mode, the Model 9514 Counter is periodically monitoring the ATN line. Table 1.14 lists the state of the handshake control lines in the idle mode.

1.5.4.4.2 The acceptor mode is entered whenever ATN is asserted by the controller. The interface standard requires that the instrument enters the acceptor mode within 200 μsec after ATN is asserted. Figure 1.49 shows the sequence followed when the counter enters the accept mode. Notice that $\overline{ACC}$ allows HATN to force the handshake lines (as seen by the system controller) to enter the Acceptor Ready State within a few gate delays. The processor will then have time to detect the pressure of the ATN signal. In order to proceed to accept characters from the interface, the processor changes the input lines to U25 from the idle state to the Acceptor Ready State and sets ACC low, thus gaining direct control of the bus handshake lines. Assume that the system controller proceeds to send the instrument's listen address through the bus. The Model 9514 will accept it and in doing so it will become a listener.

1.5.4.4.3 After the system controller has finished sending universal commands to all the instruments, it will have designated one talker and one or several listeners, the 9514 counter being one of them, and it will proceed to remove ATN. At this point the 9514 counter will remain in its acceptor mode and will continue to receive characters from the bus. These characters will be interpreted as device commands as opposed to universal commands which are accepted when ATN is low. All instruments not addressed by the controller will enter their idle state when ATN is removed.

1.5.4.4.4 The source mode is entered whenever ATN is high and the 9514 counter has been addressed as a talker. Figure 1.50 shows the timing of pertinent signals in the source mode. It is assumed that the 9514 counter is sending the last byte of measurement data (EDI assorted) before the controller asserts ATN and proceeds to untalk the counter. Notice that $\overline{ACC}$ is set high during the source mode allowing ATN to force the 9514 into its Acceptor Ready State as seen by the controller.

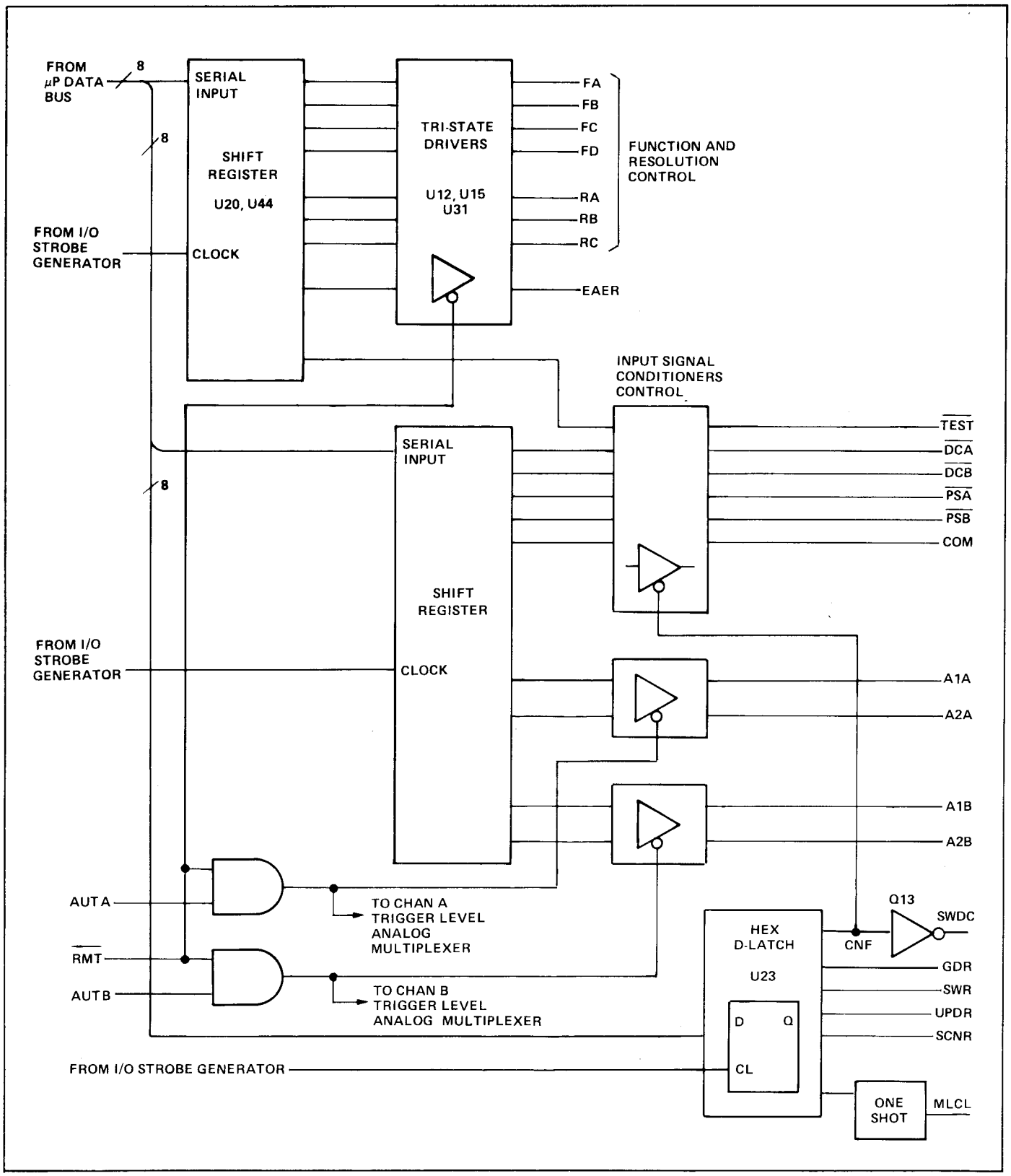


Figure 1.48 - GPIB Logic

Table 1.15 - GPIB Logic Signals

Mnemonic	Description
HATN	Inverted version of ATN. Its high state indicates that ATN was asserted by controller.
HDAVO	Set high by processor in the source mode to signal that there is data present on the GPIB. Remains low during idle or acceptor mode.
LRFDO	Set high by processor to indicate that it is not ready to receive data from the GPIB. Remains low during idle or source mode.
LDACO	Set high by processor to indicate that it has not accepted data from the GPIB. Remains low during idle or source mode.
END	Set high by processor in the source mode to indicate end of transmission. Line set high during the handshake of last character.
LDEN	Set low to enable the buffers for transmitting data onto the GPIB.
DO1 - DO7	Data output lines from the processor to GPIB. Data is not placed on the GPIB until the buffers are enabled by LDEN.
$\overline{\text{ACC}}$	Set high by processor in the source and idle modes. It allows ATN to place bus in the acceptor mode (as seen from the outside) within 200 nsec as required by the IEEE 488-1975 standard. Once the processor detects that ATN has been asserted, it proceeds to accept characters after setting ACC low.
HSRQ	Set high by processor to indicate to the controller of the GPIB that the 9514 Counter requires service.
LSRQ	Inverted version of HSRQ to light SRQ LED on front panel.
$\overline{\text{LISTEN}}$	Signal to front panel to indicate LISTEN mode.
$\overline{\text{TALK}}$	Signal to front panel to indicate TALK mode.
$\overline{\text{RMT}}$	Signal to front panel and main logic of counter to indicate REMOTE operation (i.e. front panel control inactive).
DI1 - DI7	Inverted version of data lines DI01 - DI07 on the GPIB.
HREN	Inverted version of REN on the GPIB.
HIFC	Inverted version of IFC on the GPIB.
LRFDI	Inverted version of NRFD on the GPIB.
HDAVI	Inverted version of DAV on the GPIB.
LDAC	Inverted version of NDAC of the GPIB.
AD1 - AD5	Signals from address switch. They indicate the user's selection of address for the counter. Presented in inverted logic to the processor. A closure to ground (switch "on") indicates a logic one.
TON	Talk only signal from back panel DIP switch. When low (switch "on") indicates that interface must go into source mode.

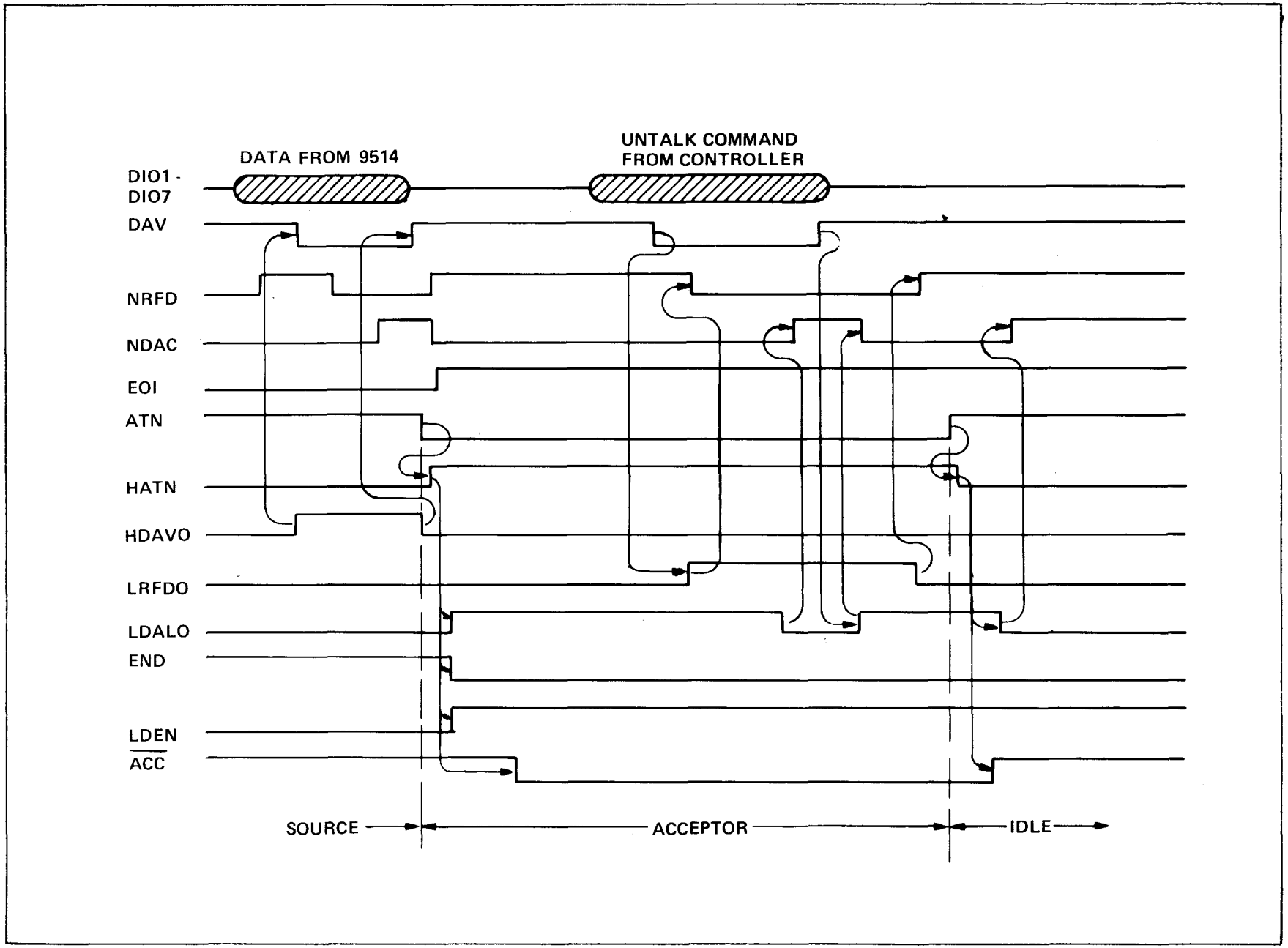


Figure 1.49 - Acceptor Mode Timing Diagram

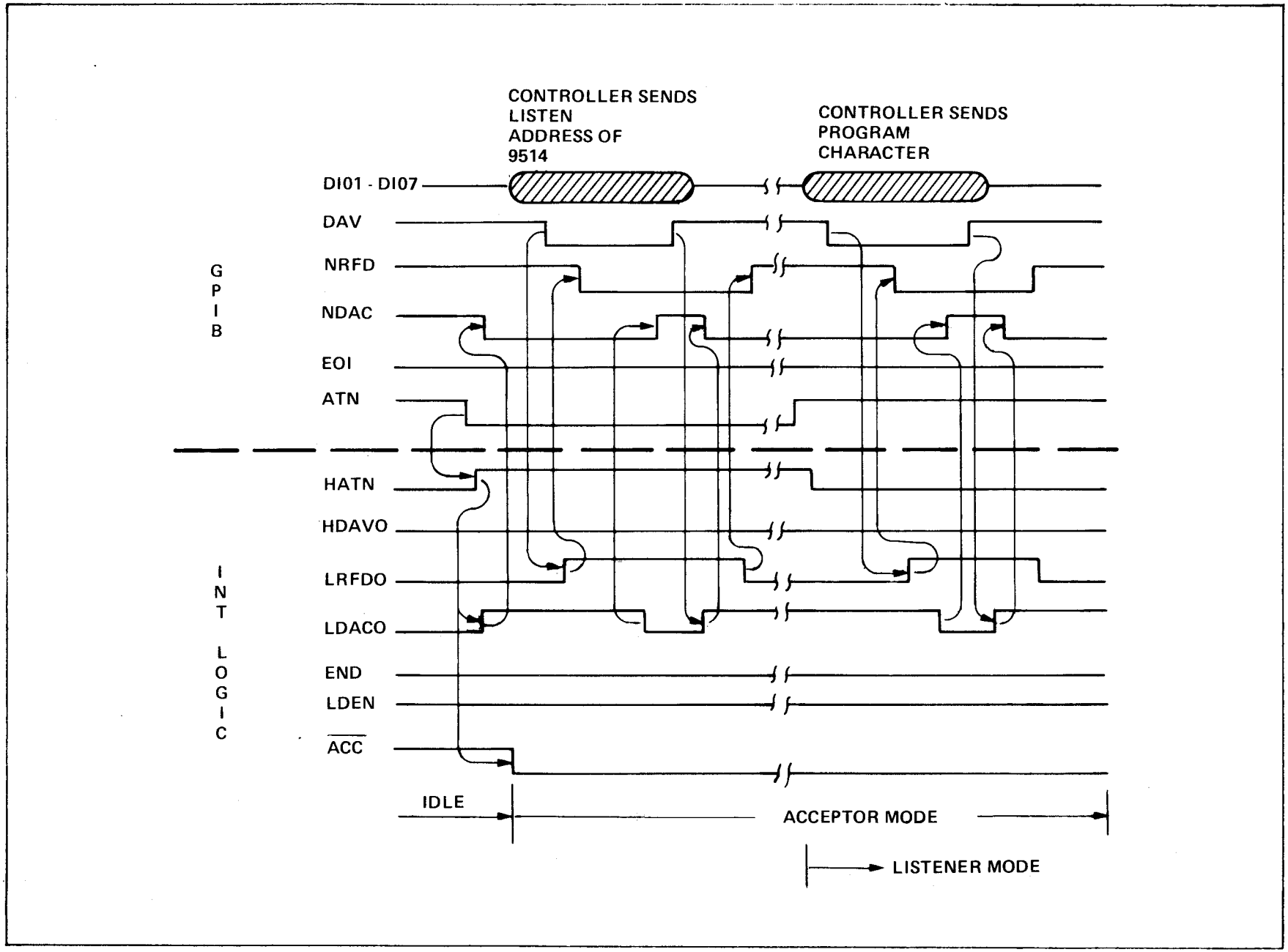


Figure 1.50 - Source Mode Timing Diagram

SECTION 2 MAINTENANCE

2.1 INTRODUCTION

2.1.1 This section contains the information necessary to check the calibration, perform calibration adjustments, and to troubleshoot the Series 9500 Counter/Timer in case of malfunction. The calibration checks are also used for receiving inspection or specification validation purposes.

2.1.2 This section is divided into three major subsections: (1) Calibration Checks, (2) Calibration Adjustment and (3) Troubleshooting Performance Tests. The troubleshooting performance tests are divided by function and are designed to enable isolation of a malfunction to a replaceable module, subassembly, or an individual component or circuit.

2.2 CALIBRATION CHECKS

2.2.1 This subsection of the Maintenance section contains instructions and reference information for checking the calibration of the Series 9500 Counter/Timer. The instructions are presented in tabular form and are organized by instrument function. In addition, the test setup, input, and control settings are provided for each step in the procedure. The test equipment required for calibration is listed in table 2.1. The calibration checks are listed in table 2.2.

2.2.2 The following steps must be performed before the calibration procedure is started.

a. Check line voltage.

b. Verify that proper voltage and fuse rating have been chosen for the instrument. If the instrument is equipped with an optional reference oscillator, check the option power supply line selector.

c. Connect the power cord to the line. Set the power switch (PWR) to ON and provide 1/2 hour for temperature stabilization.

d. Refer to the operating manuals provided with the calibration equipment to be used and provide appropriate warmup time as required.

e. Review the calibration procedure and verify that all necessary equipment and hardware are assembled.

Table 2.1 - Required Equipment

NOTE

Minimum use specifications are the principal parameters required for performance of the calibration and are included to assist in the selection of alternate equipment. Satisfactory performance of alternate items shall be verified prior to use. All applicable equipment must bear evidence of current calibration.

Item	Minimum Use Specification	Calibration Equipment
1. Frequency Standard	1 MHz, 5 MHz or 10 MHz	
2. Oscilloscope	100 MHz Bandwidth	Tektronix 454
3. Voltmeter	4-digit accuracy, 10 MΩ or greater input resistance	Data 4200
4. Signal Generator	100 Hz – 100 MHz 1V adjustable	HP651B HP8654A
5. Signal Generator	100 MHz – 512 MHz	HP8654A
6. Square Wave Generator	50V P.P. @ 10 kHz	Tektronix 105
7. Alignment Tool	Blade (non-metallic)	General Cement 9300
8. BNC T-Connector		
9. Sampling Voltmeter	0 – 1.25 GHz	HP3406
10. Pulse Generator	8 ns pulse width	Datapulse 112 or 110B or Systron-Donner 114A
11. Three cables with BNC connectors		
12. 50-Ω BNC Termination		
13. Sweep Oscillator	50 MHz – 1.25 GHz	HP8620A with HP8622A RF plug-in
14. Attenuator	1.25 GHz	HP 8495A

Table 2.2 - Calibration Checks

Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
Press and hold RESET switch.	Digit and decimal point display LED		All eights and decimal points displayed.
FUNCTION: FA N/RESOLUTION: 0	Annunciators		MHz
N/RESOLUTION: 4	Annunciators		kHz
N/RESOLUTION: 6	Annunciators		Hz
FUNCTION: P N/RESOLUTION: 0	Annunciators		μs
N/RESOLUTION: 2	Annunciators		ms
N/RESOLUTION: 4	Annunciators		sec
FUNCTION: PA N/RESOLUTION: 6	Annunciators		ns
FUNCTION: FA N/RESOLUTION: 100 Hz RANGE: 1 TEST/COM/SEP: COM SAMPLE RATE: Maximum CCW without setting to HOLD INPUT CONTROLS: A B Slope + – AC/DC AC AC Trigger Level PRE-SET PRE-SET Apply a 25 mVrms, 1 MHz signal to INPUT A.	 INPUT A Sensitivity		 1000.0 kHz
Adjust the input signal to 30 MHz, 50 mVrms.	INPUT A Sensitivity		30 000.0 kHz
Adjust the input signal to 100 Mhz, 100 mVrms.	INPUT A Sensitivity		100 000.0 kHz
Apply a 25 millivolt, 1 MHz signal to INPUT B.	INPUT B Sensitivity		1000.0 kHz

Table 2.2 - Calibration Checks continued

Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
Adjust the input signal to 30 MHz, 50 mVrms	INPUT B Sensitivity		30 000.0 kHz
Adjust the input signal to 100 MHz, 100 mVrms	INPUT B		100 000.0 kHz
If the 512 MHz Direct Count Option (41) is installed in channel C, apply a 15 millivolt, 50 MHz signal to INPUT C. FUNCTION: Fc N/RESOLUTION: 1 MHz			50 MHz
Adjust the input frequency to 512 MHz			512 MHz
If the 1.25 GHz Option (42) is installed in channel C, apply a 30 millivolt, 50 MHz signal to INPUT C. FUNCTION: Fc N/RESOLUTION: 1 MHz			50 MHz
Using the sweep oscillator and attenuator, apply a −17 dBm, 1.25 GHz signal to INPUT C. Measure the input signal with the sampling voltmeter.			1250 MHz
If the Analog Trigger Level output option is installed, connect a DC voltmeter between the GND connector and the A connector on the rear panel. Rotate the INPUT A trigger level control from fully CW to fully CCW without setting to the PRESET position.	Analog Trigger Output A		Greater than +3 volts at CW end and more negative than −3 volts at the CCW end.
Connect the voltmeter between the GND connector and the B connector on the rear panel. Rotate the INPUT B trigger level control from fully CW to fully CCW without setting to the PRESET position.			Greater than +3 volts at CW end and more negative than −3 volts at the CCW end.

Table 2.2 - Calibration Checks continued

Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
If the Analog Trigger Option is not installed perform the following procedure: Loosen the four captive screws and lift off the top cover of the counter.			
Connect a DC voltmeter between TP2 (GND) and E6 for the Model 9514 counter and between TP5 on mother board (ground) and E3 on switch board for Model 9510. Rotate the INPUT A and INPUT B trigger level controls fully CW.		Figure 2.1 for 9510 Figure 2.2 for 9514	Greater than +3 volts.
Move the voltmeter high lead to E5 (9514) or E5 (9510)		Figure 2.1 for 9510 Figure 2.2 for 9514	Greater than +3 volts.
Rotate the trigger level controls fully CCW without setting them to PRESET.		Figure 2.1 for 9510 Figure 2.2 for 9514	More negative than –3 volts.
Move the voltmeter high lead to E6.		Figure 2.1 for 9510 Figure 2.2 for 9514	More negative than –3 volts.
FUNCTION: TOT TEST/COM/SEP: TEST INPUT A Trigger Level: PRESET INPUT B Trigger Level: PRESET Press the START switch	Totalize		Verify that the counter is counting.
Press the STOP switch			Verify that the counter stops counting and displays the accumulated count.
Press the START switch and allow the counter to run for more than 100 seconds.	Overflow		The OF (overflow) indicator should light.

Table 2.2 - Calibration Checks continued

Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
FUNCTION: P N/RESOLUTION: 0	Period		0.1 μs
FUNCTION: PA N/RESOLUTION: 2	Period Average		100 ns
FUNCTION: B/A N/RESOLUTION: 2	Ratio of B to A		1.00
If 512 Direct Count RF board is installed: FUNCTION: C/A TEST/COM/SEP: COM Apply a 50 millivolts, 100 MHz signal to INPUT C. Apply a 1 KHz signal to INPUT A.	Ratio of C to A		100 000.0
FUNCTION: C/A→B	Counts of C in the interval from A to B		50 000.0
FUNCTION: TI N/RESOLUTION: 0 TEST/COM/SEP: COM INPUT CONTROLS: A B Slope + – AC/DC AC AC Trigger Level PRE-SET PRE-SET Apply a 100 kHz signal 1 Vrms signal to INPUT A.	Time Interval		5.0 μsec
FUNCTION: TIA N/RESOLUTION: 3	Time Interval Average		5000.0 nsec
FUNCTION: F_B N/RESOLUTION: 5 Using an oscilloscope, monitor the GATE OUT signal on the rear panel.	GATE OUT		100 ms TTL positive going pulse equal to the width of the measurement gate.

Table 2.2 - Calibration Checks continued

Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
FUNCTION: TI TEST/COM/SEP: COM RANGE: 1 INPUT CONTROLS: A B Slope + – AC/DC AC AC Trigger Level PRE-SET PRE-SET Apply a 1 kHz signal to INPUT A and monitor the MARKER OUT signal on the rear panel.	MARKER OUT		.5 ms negative going signal 
Monitor the REF signal on the rear panel.			10 MHz reference signal.
FUNCTION: FA N/RESOLUTION: 7 TEST/COM/SEP: COM INPUT CONTROLS: A B Slope + – AC/DC DC DC Trigger Level PRE-SET PRE-SET Connect a 1 MHz frequency standard to INPUT A.	Internal Reference Frequency		The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following equation: Internal Oscillator Frequency = 10 (2,000,000.0 – counter display) Some examples of various counter readings and the frequency difference that is indicated are shown as follows:

Table 2.2 - Calibration Checks continued

Input and Control Setting	Function Tested	Illustration Reference	Performance Standard	
			Counter Display	Internal Reference Osc.
			999 995.0 Hz	10,000.050 kHz
			999 997.5 Hz	10,000.075 kHz
			1000 000.0 Hz	10,000.000 kHz
			1000 002.5 Hz	9,999.975 kHz
			1000 005.0 Hz	9,999.950 kHz
FUNCTION: FA TEST/COM/SEP: TEST N/RESOLUTION: 5 REF INT/EXT: EXT (Rear Panel) Apply a 10 MHz external reference standard to the REF connector on the rear panel. If the Reference Multiplier option is installed, 1, 5, or 10 MHz may be used.	External Reference Frequency		10000.00 kHz	
FUNCTION: FA N/RESOLUTION: 3 TEST/COM/SEP: TEST GATE DELAY: A⌐¬B (Left) (Rear Panel) Connect a cable between the oscilloscope B+ GATE connector and the rear panel GATE CONTROL connector. Connect a cable between the oscilloscope CH A input and GATE OUT on the rear panel. Set oscilloscope controls as follows: HORIZ DISPLAY: A INTEN DURING B B SWEEP MODE: B STARTS AFTER DELAY TIME	Gate Delay	Figure 2.3		

Table 2.2 - Calibration Checks continued

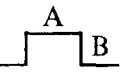
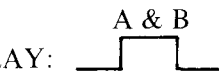
Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
DELAYED SWEEP: 50 μs A TIME/DIV: 1 ms A SWEEP MODE: NORM TRIGGER SLOPE: + Adjust the DELAY TIME MULTIPLIER to set the intensified portion of the trace on the falling edge of the waveform.			Waveform 1 Waveform 2 When the intensified trace is on the falling edge of the GATE signal, the measurement gate closing is delayed by 1 ms. Counter displays 20.000 MHz.
FUNCTION: TI GATE DELAY:  TEST/COM/SEP: COM N/RESOLUTION: 0 INPUT CONTROLS: A B Slope + – AC/DC AC BC Trigger Level PRE-SET PRE-SET Connect the pulse generator pulse output connector to INPUT A on the counter and channel 1 on the oscilloscope using a BNC T-connector. Connect the pulse gènerator sync out to the oscilloscope external trigger. Connect the counter GATE CONTROL to the oscilloscope B+ GATE connector.	Selective Gate	Figure 2.4	

Table 2.2 - Calibration Checks continued

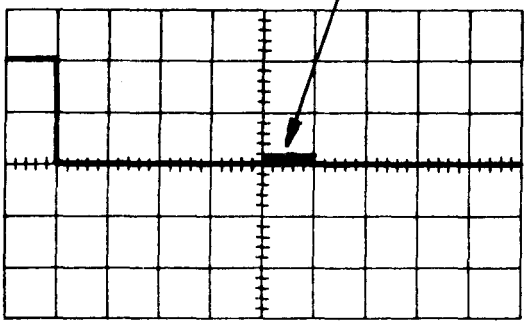
Input and Control Setting	Function Tested	Illustration Reference	Performance Standard
Set the pulse generator as follows: Rep Rate: ≃170 Hz Pulse Mode: double Delay: ≈1 ms Width: ≈1 ms Amplitude: 2 volts Pulse Polarity: + Gate Mode: non-gated Set the oscilloscope as follows: HORIZ DISPLAY: A INTEN DURING B B SWEEP MODE: B STARTS AFTER DELAY TIME DELAYED SWEEP: .2 μs A SWEEP MODE: NORM TRIGGER EXT TRIG: + SLOPE			Waveform 3 Counter displays the time between channel A trigger and channel B trigger.
Adjust the oscilloscope DELAY TIME MULTIPLIER to encircle the pulse with the intensified trace.			Waveform 4
A & B GATE DELAY:  N/RESOLUTION: 1 FUNCTION: TIA Adjust the DELAY TIME MULTIPLIER to encircle the pulse with the intensified trace.	Synchronous Window		Waveform 5 Counter displays the time interval covered by the intensified trace in waveform 5.
Adjust the DELAY TIME MULTIPLIER as shown in waveform 6.			Waveform 6 No counter reading.
If the rear panel input option is installed, connect a 300 millivolt input signal to FA, FB, and FC in turn.	Rear Panel Inputs		Verify frequency on display.

Waveforms for Table 2-2

1 (NO.)

GATE OUT

INTENSIFIED TRACE

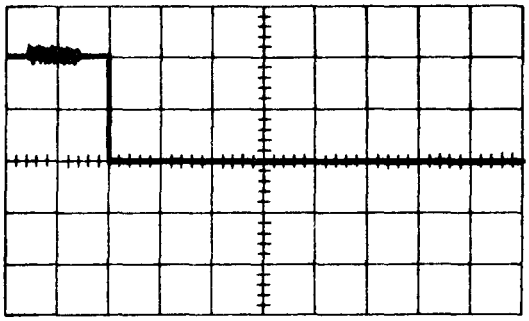


1 (V/DIV)

1 mS (S/DIV)

2 (NO.)

GATE OUT

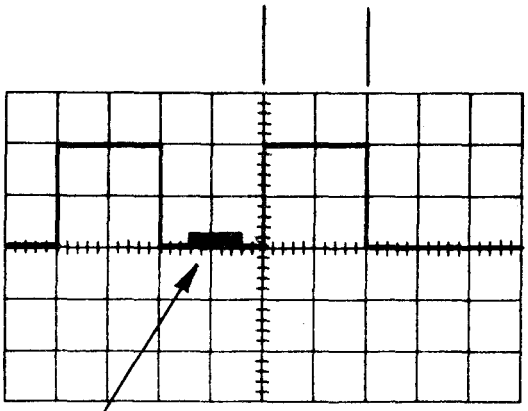


1 (V/DIV)

1 mS (S/DIV)

3 (NO.)

TIME MEASURED BY COUNTER



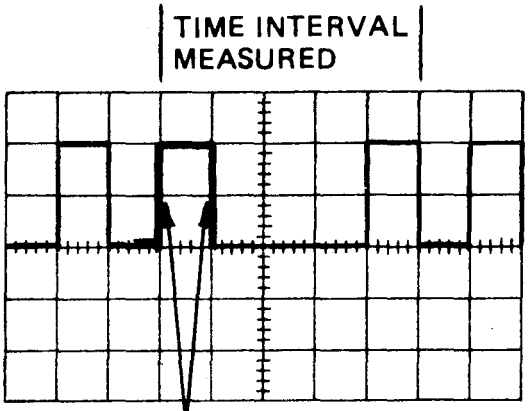
1 (V/DIV)

INTENSIFIED TRACE

0.5 mS (S/DIV)

4 (NO.)

TIME INTERVAL MEASURED



1 (V/DIV)

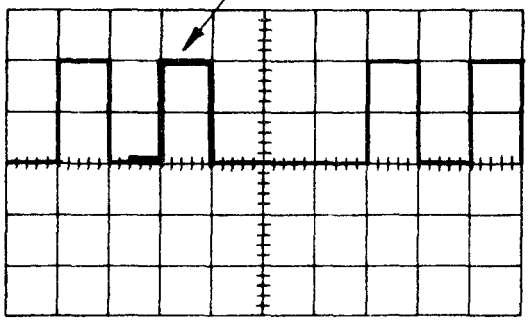
INTENSIFIED TRACE

1 mS (S/DIV)

5 (NO.)

TIA READING

INTENSIFIED TRACE



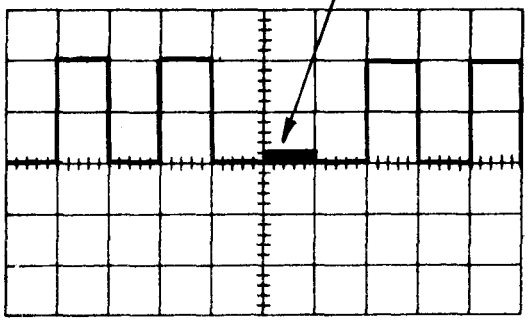
1 (V/DIV)

1 mS (S/DIV)

6 (NO.)

NO COUNTER READING

INTENSIFIED TRACE



1 (V/DIV)

1 (S/DIV)

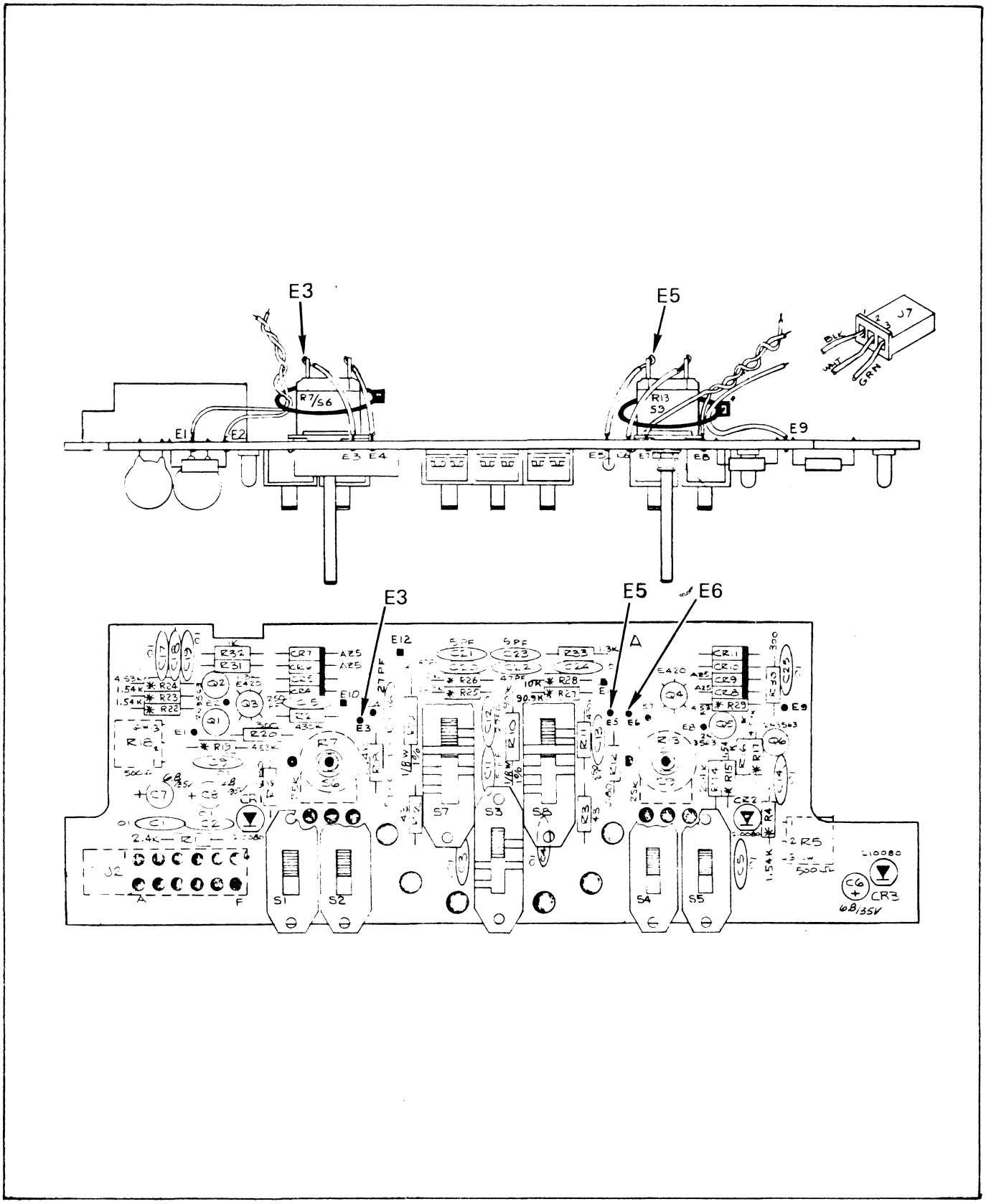


Figure 2.1 - Trigger Level Control Measurement Locations

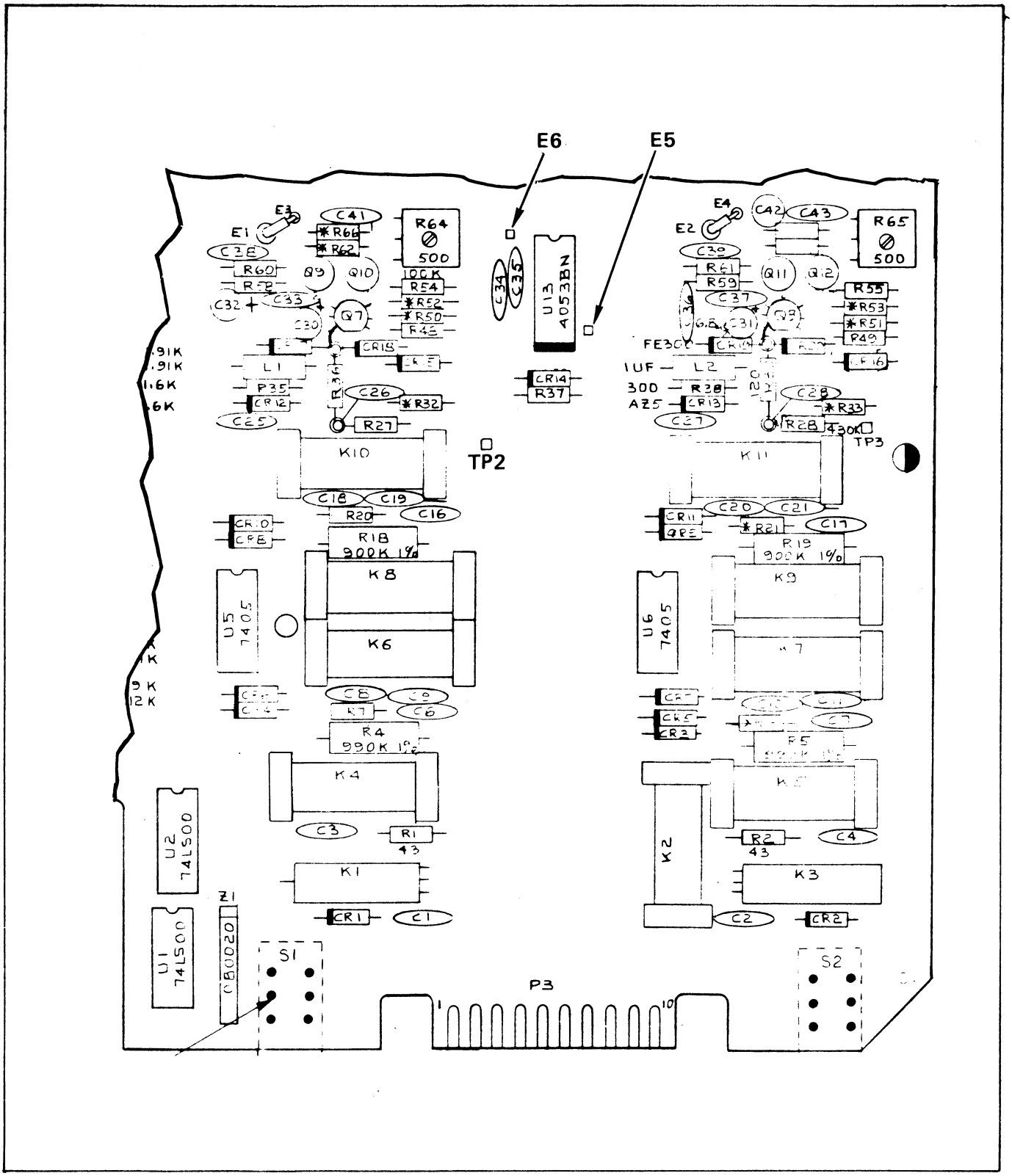


Figure 2.2 - Trigger Level Control Measurement Location

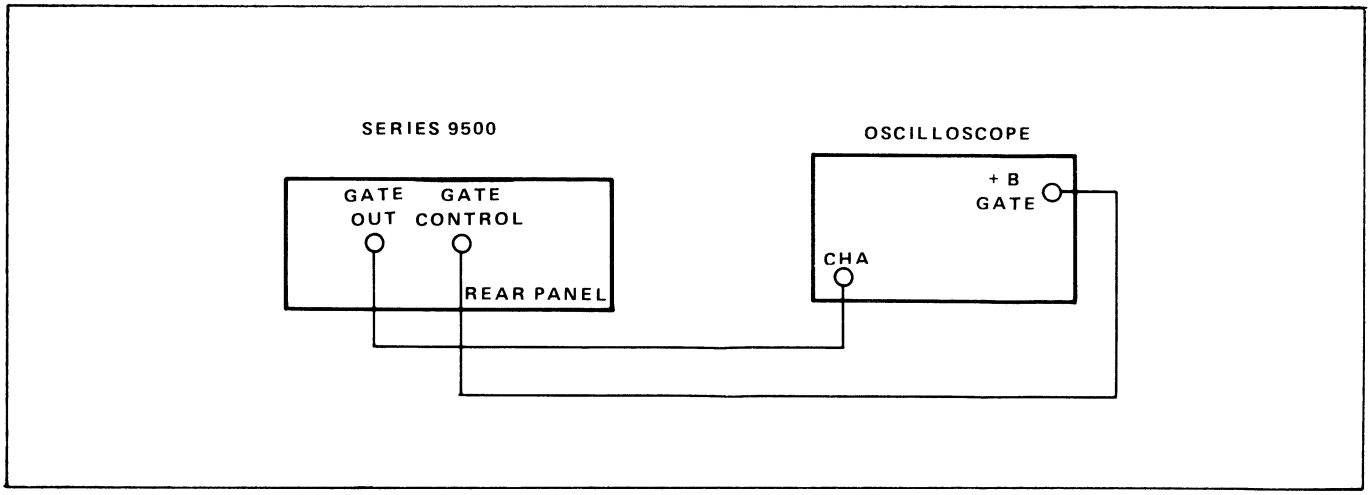


Figure 2.3 - Gate Delay Test Setup

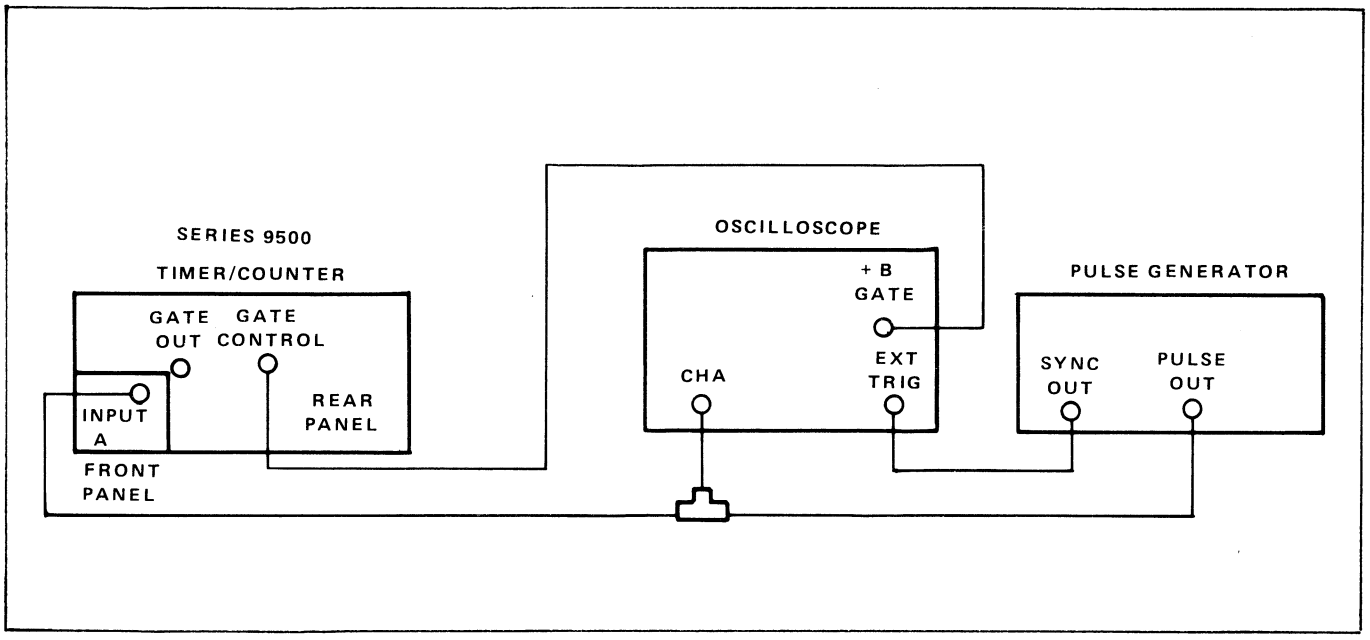


Figure 2.4 - Selective Gate Test Setup

2.2.3 GPIB Assembly Calibration Check

2.2.3.1 In order to perform operational and calibration checks on the GPIB assembly of the Model 9514 counter/timer a controller is needed to exercise the various circuits and control functions. In the following paragraphs the HP9825A calibrator with the advanced programming and extended I/O options was used. A listing of the programs is provided along with a description of their function.

2.2.4 DAC Calibration Check

2.2.4.1 If the instrument is equipped with the analog trigger level output option, the DAC output may be measured at the rear terminals marked A, B, and ⏚. These terminals are located by the left upper corner of the back of the instrument, close to the MARKER OUT BNC. If the analog trigger level output option is not installed, remove the top cover of the instrument. The trigger level for channel A may be measured at test point "E6", while channel B trigger level is present at test point "E5".

2.2.4.2 To check calibration of the digital-to-analog converter for channel A execute the program lines on the HP9825A calculator as indicated on table and measure test points E6 and E5 with respect to ground (TP2).

Program Line	Voltage Measurements E5 to GND, E6 to GND
wrt 700, "LA+300 LB +300"	+3.00 volts ± 12.5 mV
wrt 700, "LA-300 LB-300"	-3.00 volts ± 12.5 mV

UNIVERSAL COMMAND TEST

```
0: lcl 7;rem 7;
 rem 700;clr
 700;cmd 7,"?";
 flt 9
1: dsp "REMOTE";
 stp
2: cmd 7,"@";
 dsp "TALK";stp
3: cmd 7," ";
 dsp "LISTEN";
 stp
4: wrt 700,"RC2S
 1T";dsp "SRQ";
 stp
5: clr 700;cmd
 7,"?";dsp "PRES
 S RESET ON COUN
 TER";wait 3000
6: dsp "IF COUNT
 ER IN LOCAL,
 CONTINUE";stp
7: clr 700;cmd
 7,"?";llo 7
8: dsp "PRESS
 RESET ON COUNTE
 R";wait 3000
9: dsp "IF COUNT
 ER IN REMOTE,
 CONTINUE";stp
10: lcl 700;cli
 7;dsp "IF COUNT
 ER IN LOCAL;
 END OF TEST";
 stp
*29071
```

The program shown on the left performs a test on the response of the counter to universal commands. After each command is issued, the program stops execution while the user verifies that the proper annunciators are lighted on the front panel. To resume execution, the user must press the CONTINUE key on the calculator.

Figure 2.4A - Universal Command Test

DEVICE COMMANDS TEST

```
0: dim A$[20],
 B$[20],C$[20],
 D$[20]
1: wrt 700,"RC2F
 0"
2: rds(700)→A
3: if A#2;prt
 "STATUS BYTE
 ERROR;R/C2/F0/
 ";stp
4: red 700,A
5: if A#1e7;prt
 "MEASUREMENT
 DATA ERROR;R/
 C2/F0"
6: for I=0 to 7
7: "G"&char(I+
 48)→D$
8: wrt 700,D$
9: red 700,A$
10: A$[1,11]→B$
11: A$[13,15]→C$
12: val(B$)→B;
 val(C$)→C
13: if 1e-8*10↑I
 -B#0;sto "RER"
14: if 15-I-C#0;
 sto "RER"
15: jmp 2
16: "RER":prt
 "RES. SETTING
 OR DATA OUT
 ERROR",D$;stp
17: next I
18: end
*19110
```

N/RESOLUTION Test

The program shown on the left checks the programming of the N/RESOLUTION modes of the instrument. No input signals are needed since the internal 10 MHz signal is used throughout the program. In case of an error a message is printed, followed by the command(s) that failed to produce the expected response from the instrument.

Figure 2.4B - Device Commands Test

FUNCTION COMMANDS TEST

```
0: dim A$[20],
 B$[20],C$[20]
1: spc 2;flt 9
2: prt "IS OPTIO
 N   41   INSTAL
 LED?"
3: prt "ENTER Y
 OR N &"
4: prt "PRESS
 CONTINUE"
5: ent B$
6: B$[1,1]→B$
7: cap(B$)→B$
8: if B$="Y";
 1→A;jmp 2
9: 0→A
10: "RF0C2"→A$
11: gsb "PR"
12: if B#1e7;
 gto "ERR"
13: "F2G4"→A$
14: gsb "PR"
15: if B#1;gto
 "ERR"
16: "F4G0"→A$
17: gsb "PR"
18: if B#1e-7;
 gto "ERR"
19: "F6G4"→A$
20: gsb "PR"
21: if B#1e-7;
 gto "ERR"
22: "F8G0"→A$
23: gsb "PR"
24: if B#1e7;
 gto "ERR"
25: "F:PV"→A$
26: gsb "PR"
27: if B=0;gto
 "ERR"
28: "F4G0C1LAALB
 A"→A$
29: gsb "PR"
30: B→P
31: "F5"→A$
32: gsb "PR"
33: if abs(P/B-
 2)>.2;gto "ERR"
34: "F7G3"→A$
35: gsb "PR"
36: B→T
37: if abs(P/T-
 2)>.2;gto "ERR"
38: if A=0;gto
 "Z"
39: "F1G6"→A$
40: gsb "PR"
41: B→C
42: if abs(C-
 1e8)>1e7;gto
 "ERR"
43: "F3G0"→A$
44: gsb "PR"
45: if abs((B-C*
 P)/(C*P))>.2;
 gto "ERR"
46: "F9"→A$
47: gsb "PR"
48: if abs((B-C*
 T)/(C*T))>.2;
 gto "ERR"
49: "Z":end
50: "PR":wrt
 700,A$
51: red 700,B
52: ret
53: "ERR":prt
 "ERROR";prt A$;
 dsp "LAST COMMA
 ND(S): ",A$
54: end
*20446
```

The program shown above executes a test of all measurement functions. Before running the program, the following signals must be connected to the instrument.

Channel A: 1 kHz, sine wave, 1 Vrms
Channel C (Option 41): 100 MHz, sine wave, 50 mVrms

The program will step the instrument through all its functions. In case of an error message is printed followed by the command(s) that failed to produce the expected response.

Figure 2.4C - Function Commands Test

2.3 CALIBRATION ADJUSTMENTS.

2.3.1 Test setup and adjustment instructions are presented in this subsection. If performance of the calibration checks indicate the need for adjustment, perform the appropriate adjustment procedure. Like the calibration checks, the adjustment procedures are organized by instrument function. This section covers the calibration of the Dana Series 9500 Timer/Counter and is designed to return the instrument to its published specification for indefinite periods of time. The procedure consists of applying known input levels and adjusting the appropriate component for the indicated value. A list of equipment required to perform the calibration procedure is provided in table 2.1.

2.3.2 Disassembly of the instrument case is as follows:

a. Place instrument on a flat level surface with the bail extended towards the back of the instrument.

b. Disconnect the power cable and loosen the captive screws on the top cover.

2.3.3 The following steps are performed prior to making any adjustments to the instrument.

a. Check the line voltage requirements stamped on the serial tag located on the back of the instrument and insure that the available power source is the same. Connect the instrument to the line and set the power switch to ON. Allow at least 30 minutes for the instrument to temperature stabilize.

b. Refer to the operating manuals provided with the test equipment to be used and provide appropriate warmup time.

> **WARNING**
>
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

2.3.4 The calibration points are located on the main logic board and the GPIB board (9514 only).

2.3.5 The order of adjustment has been determined to produce the least interaction between adjustments. For best results, the procedure should be followed as presented.

2.3.6 Signal Conditioners

2.3.6.1 SENSITIVITY

a. Preset the operating controls as follows:

FUNCTION: FA

N/RESOLUTION: 1 Hz

TEST/COM/SEP: SEP

RANGE: X1

INPUT CONTROLS:

	A	B
Slope	+	–
AC/DC	DC	DC
Trigger Level	PRESET	PRESET

SAMPLE RATE: Maximum CCW without setting to HOLD.

b. Apply a 1V RMS, 100 Hz signal to the channel A input connector and verify a reading of 100 Hz.

c. Reduce input voltage until no gating occurs.

d. Toggle the channel A slope switch between + and – and adjust potentiometer R18 (9510) or R64 (9514) for proper display in both + and – slope with the least amount of input signal.

e. Select FB and common mode. Set input to 1V RMS and verify a counter display of 100 Hz.

f. Reduce input voltage until no gating occurs.

g. Toggle the channel B slope switch between + and – and adjust potentiometer R5 (9510) or R65 (9514) on channel B signal conditioner for a proper display in both + and – slope with the least amount of input signal.

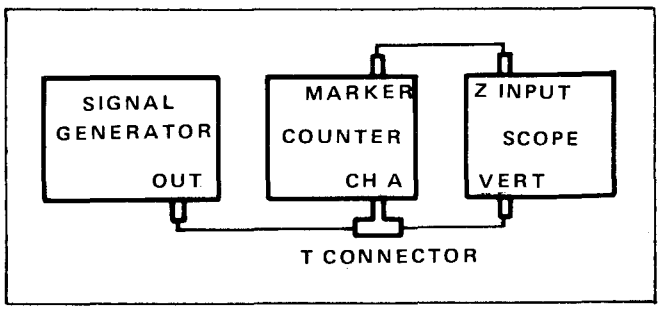


Figure 2.5 - Marker Hookup

2.3.6.2 HYSTERESIS COMPENSATION

a. Preset the operating controls as follows:

FUNCTION: TI

N/RESOLUTION: 5

TEST/COM/SEP: COM

RANGE: X1

INPUT CONTROLS:

	A	B
Slope	+	–
AC/DC	DC	DC
Trigger Level	PRESET	Slightly CCW but not enough to inhibit gating

b. Apply a 100 Hz @ .3V P.P. signal to the channel A input and the oscilloscope vertical input; connect the marker output on the back of the counter to the oscilloscope Z axis (see figure 2.5).

c. Toggle the channel A slope switch between + and – and adjust potentiometer R54 on the main logic board for the same trigger levels at both positions of the slope switch.

d. Adjust R18 (9510) or R64 (9514) for a trigger point of zero volts.

e. Set Channel A trigger level control slightly CW from center but not eough to inhibit gating. Set channel B trigger level to PRESET.

f. Toggle the channel B slope switch between + and – and adjust potentiometer R85 on the main logic board for the same trigger levels at both positions of the slope switch.

g. Adjust R5 (9510) or R65 (9514) for a trigger point of zero volts.

h. Set the FUNCTION switch to A/B and the N/RESOLUTION switch to 6. Set the trigger level on channel A and channel B to PRESET.

i. Apply a 100 mV RMS, 100 MHz signal to the channel A input connector and verify a counter display of 1.000000.

2.3.7 Internal Reference

2.3.7.1 There are three internal reference oscillators available for the Series 9500. (See table 2.3.)

2.3.7.2 The calibration adjustment for the standard oscillator is a single variable capacitor adjustment, accessible at the rear panel (OSC ADJ). The

Table 2.3 - Internal Reference Oscillators

Oscillator	Aging Rate	Temperature Stability	Stability
Standard	$<3\times10^{-7}$/mo.	$<5\times10^{-6}$ 0°C to +50°C	$<1\times10^{-7}$ with 10% line V variation
Option 22	$<1\times10^{-9}$/day	$<5\times10^{-9}$ 0°C to +50°C	$<2\times10^{-9}$ with 10% line V variation
Option 24	$<1\times10^{-10}$/day	$<5\times10^{-9}$ 0°C to +50°C	$<2\times10^{-9}$ with 10% line V variation

options have two adjustments (COARSE and FINE), accessible at the rear panel.

2.3.7.3 REFERENCE OSCILLATOR FREQUENCY CHECK

a. Select the following control settings:

FUNCTION	F_A
N/RESOLUTION	7
CHANNEL A	
Slope	+
AC/DC	DC
Trigger Level	PRESET
SEP/TEST/COM	COM

b. Connect the 1 MHz frequency standard to the channel A input.

c. The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following equation:

Internal Oscillator Frequency = 10x(2,000,000.0 - Counter Reading).

d. Some examples of various counter readings and the frequency difference that is indicated are shown below:

Counter Display	Internal Reference Osc.
999 994.0 Hz	10,000.050 kHz
999 997.5 Hz	10,000.075 kHz
1000 000.0 Hz	10,000.000 kHz
1000 002.5 Hz	9,999.975 kHz
1000 005.0 Hz	9,999.950 kHz

2.3.7.4 ADJUSTMENT PROCEDURE

a. Connect the 1 MHz 1V RMS frequency standard to the vertical input of the oscilloscope.

b. Connect the REF signal from the rear panel of the counter to the external trigger of the oscilloscope.

c. Set the oscilloscope controls as follows:

TRIGGER	
SLOPE:	+
COUPLING:	AC
SOURCE:	EXT
SWEEP MODE	
NORM	
TRIGGER	
SWEEP:	0.05 μS
CHANNEL INPUT:	AC
volts/div	Depends on amplitude of frequency standard
TRIGGER LEVEL:	center of mechanical span

d. Adjust the scope's trigger level for a trace display of the frequency standard output.

e. If the instrument is equipped with the standard reference oscillator, adjust OSC ADJ for an oscilloscope display that is as stationary as possible (does not drift to the left or right).

f. If the instrument is equipped with option 22 or 24 high stability reference oscillator, remove the protective cover in the back panel. Using the two exposed controls, perform the procedure outlined in step e.

g. To determine the drift rate of the calibrated instrument, measure the time it takes the oscilloscope pattern to drift 5 divisions on the oscilloscope. The oscilloscope drift can be determined from figure 2.6.

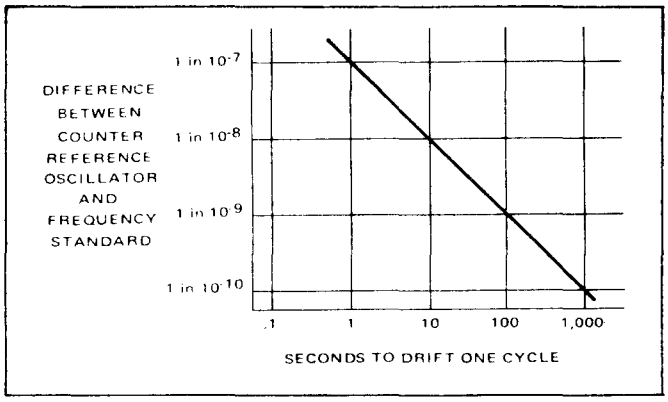


Figure 2.6 - Oscillator Drift

2.3.8 512 MHz RF Option

2.3.8.1 SENSITIVITY

a. Select the following control settings:
FUNCTION: Fc
N/RESOLUTION: 100 Hz

b. Connect a 520 MHz signal from a signal generator or sweep oscillator to the Channel C input and set the signal level to less than 5 mV RMS.

c. Remove the instrument top cover and set pot R15 on the 512 MHz RF board to its full ccw position.

d. Increase the signal level until the displayed frequency is stable.

e. Slowly turn R15 clockwise until the counter stops gating.

2.3.9 Maintenance Disassembly

2.3.9.1 Always disconnect the power cord from the instrument when disassembling beyond the calibration stage or when boards are to be removed. Power may be restored to the instrument with boards removed for troubleshooting purposes without damage to the instrument. Also remove power before inserting boards.

2.3.9.1.1 Tools Required. Besides a phillips screwdriver the following tools may be required depending on what is to be disassembled.

2.3.9.1.2 When reassembling the instrument after maintenance check for correct position of all interconnecting cables and plugs. Location and orientation of each connector may be verified on the PC board silkscreen or on the appropriate assembly drawing.

Name	Suggested Type
1. Long nose pliers	–
2. Soldering iron	35 watt
3. Solder	Rosin Core
4. Solder remover	Solda Pult

2.3.9.2 REPLACING FRONT PANEL LEDs

a. Lay the counter on its side. Loosen the four captive corner screws on the bottom cover and remove cover. Repeat the process on the top cover.

b. Remove the four button head phillips screws holding the front panel to the bottom frame.

c. Remove the four button head phillips screws holding the front panel to the top frame.

d. Remove all front knobs and on 9510 unplug P6 and P7 from mother board.

e. Press front panel assembly out from case.

f. Remove 4 phillips screws mounting display board to front panel and separate. LED devices are unsoldered for removal.

2.3.10 Board Revision

2.3.10.1 Every effort is made to keep the manual concurrent with the instrument despite changes to the design, which are an inevitable adjunct of the manufacturing process. The manual is updated and periodically reprinted throughout the year. In between printings, Addendums and Errata Sheets are added to the manual if required to implement the reprinted copy.

2.3.10.2 Any design change is accompanied by an updating of a board revision. Such change could be as simple as a revised hole size or as complex as major modifications of the circuitry. The revision of a board is indicated by the letter preceding the assembly number on the board; the revision of the assembly drawing in Section 6 or on an Errata Sheet is indicated by the letter following the assembly number, located below the drawing. Comparing the revision letters can indicate how closely the drawing corresponds to the board.

2.4 TROUBLESHOOTING PERFORMANCE TESTS

2.4.1 This section contains the troubleshooting performance tests. The performance tests are designed to isolate a malfunction to a replaceable module or component. In some cases where the circuit is complex, the test is designed to isolate the malfunction to a functional area of the board.

2.4.2 The performance tests are organized by instrument function. A "singlethread" diagram is provided for each of the performance tests. These diagrams show the primary signal path through the instrument for the individual function of the instrument.

2.4.3 The performance tests contain test setup instructions, step by step instructions for monitoring the circuit under test and performance standards in the form of voltage levels or oscilloscope waveforms. In addition the tests are fully illustrated by either the "singlethread" diagrams or schematics which illustrate the test point location within the circuit under test. For ease in locating the physical test point within the instrument, pictorial drawings are provided on pages facing the schematic.

2.4.4 Test points called out in the performance tests may be actual physical test points provided as convenience test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares or diamonds. These "flags" also appear on the corresponding schematic and on the pictorial drawing in the Drawing section of this manual.

2.4.5 Note that the test points are numbered sequentially so as to start at the input of a circuit and progress to the output. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to square black test point flags 1 appearing on the assembly drawing and schematics in the Drawing Section (3). These black square test point flags indicate voltage measurement points. Similarly the alphabetic test points refer to black diamond shaped flags A appearing on the assembly drawings and schematics. The Alphabetic diamond flags indicate oscilloscope test points.

2.4.6 To apply performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors and capacitors in and around the area of malfunction.

2.4.7 Performance Test Procedure

2.4.7.1 Table 2.4 contains a list of test points located on the mother board. Corresponding to each test point is the figure reference for the location of each test point, the type of signal at that test point, the signal designation, and pertinent remarks about the signal.

2.4.7.2 Figure 2.7 shows the high and low voltage levels of the two types of logic used in the counter. The ECL type logic is mainly used in the measurement paths of the counter where higher frequencies are encountered. The TTL logic is mainly used in control type circuits where the frequency is normally below 10 MHz.

2.4.7.3 Tables 2.5 through 2.6 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements. Troubleshooting, unlike calibration, may be done with any equipment that is accurate to 5%.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

Table 2.4 - Mother Board Test Points

Test Point	Figure Reference	Type Signal	Signal Designation	Remarks
1	2.11	DC	ground, TTL	Grounding scope or DVM
2	2.11	TTL	$\overline{\text{LOAD}}$	Active low, latches 8 LS digits in display
3	2.13	TTL	RESET	Clears accumulator to display and enables counter for next cycle
4	2.8	DC	ground, Input A	Scope gnd for high frequency measurements
5	2.8	DC	ground, Input B	Scope gnd for high frequency measurements
6	2.13	TTL	CLEAR	Clears accumulator
7	2.15	DC	ground, TTL	
8	2.15	TTL	f_r	10 MHz reference signal
9	2.8	ECL	f_b	Input B signal
10	2.13	TTL	$\overline{\text{UPDATE}}$	Triggered by end of gate; loads display and starts new cycle
11	2.16	DC	ground, ECL	Scope ground for high frequency measurements
12	2.13	TTL	TB	Output of timebase decades
13	2.16	ECL		Accumulator input (before gate)
14	2.8	ECL	f_a	Input A signal
15	2.13	DC	ground, TTL	
16	2.16	ECL	$\overline{\text{GATE}}$	Low when measurement gate is open
17	2.16	DC	ground	
18	2.34	DC	+15V	
19	2.34	DC	-12V	
20	2.34	DC	ground	
21	2.34	DC	+5V	
22	2.34	DC	+5.2V	

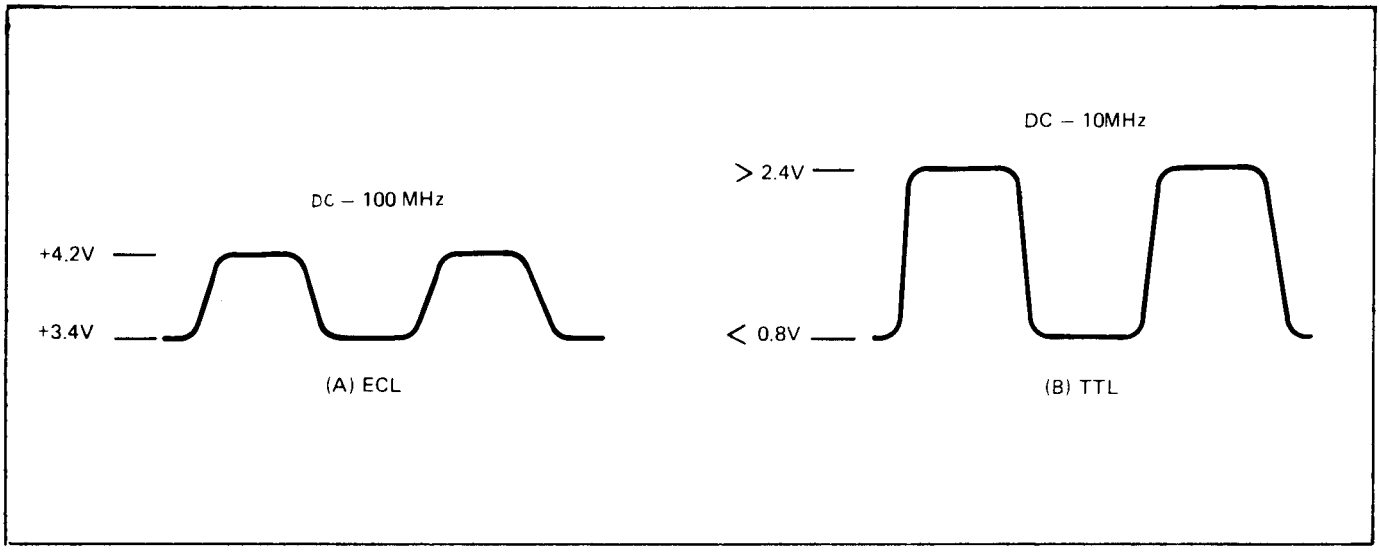


Figure 2.7 - Logic Levels

2.4.7.4 The performance tests presented in this section are:

Table 2.5 - Signal Conditioner Performance Test

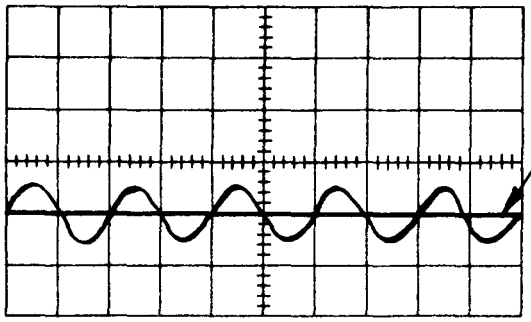
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: F A N/RESOLUTION: 4 RANGE: 1 TEST/COM/SEP: COM INPUT CONTROLS: A B SLOPE: + – AC/DC: DC DC TRIGGER LEVEL: PRESET PRESET APPLY A 1 VRMS, 10KHZ INPUT SINEWAVE TO INPUT A.		U5-8	A	Figures 2.8 & 2.9	Waveform 1
		U17-10	B	Figures 2.8 & 2.9	Waveform 2
		U17-7	C	Figures 2.8 & 2.9	Waveform 2
		TP14	D	Figures 2.8 & 2.9	Waveform 2
		U37-5	E	Figures 2.8 & 2.9	+ 3.4 Volts
Set INPUT A slope to –		U37-5	F	Figures 2.8 & 2.9	+ 4.2 Volts
		U17-3	G	Figures 2.8 & 2.9	Greater than Ø Volts.
FUNCTION: T1		U17-3	G	Figures 2.8 & 2.9	–0.7 Volts
TEST/COM/SEP: Test		U37-3	H	Figures 2.8 & 2.9	Waveform 3
Apply a 1 VRMS, 10KHz sinewave to INPUT B.		U6-8	I	Figures 2.8 & 2.10	Waveform 4
		U6-11	J	Figures 2.8 & 2.10	Waveform 4
		U18-7	K	Figures 2.8 & 2.10	Waveform 2
		U18-10	L	Figures 2.8 & 2.10	Waveform 2
		TP9	M	Figures 2.8 & 2.10	Waveform 2
		U37-11	N	Figures 2.8 & 2.10	+ 3.4 Volts
Set INPUT B slope to +		U37-11	N	Figures 2.8 & 2.10	+ 4.2 Volts
		U18-3	R	Figures 2.8 & 2.10	Greater than Ø Volts.
FUNCTION: F B		U18-3	O	Figures 2.8 & 2.10	– 0.7 Volts
TEST/COM/SEP: Test		U37-15	P	Figures 2.8 & 2.10	Waveform 3

Waveforms for Table 2.5

1 (NO.)

U5-8 SIGNAL
U5-11 TRIGGER LEVEL

INPUT A



0.5 (V/DIV)

50 µS (S/DIV)

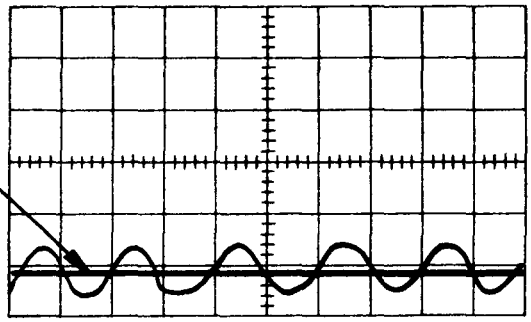
NOTE: ACTUAL DC OFFSET MAY VARY.

WHEN IN PRESET TRIGGER LEVEL MUST APPEAR THROUGH THE MIDDLE OF THE WAVEFORM

4 (NO.)

U6-8 SIGNAL
U6-11 TRIGGER LEVEL

INPUT B



0.5 (V/DIV)

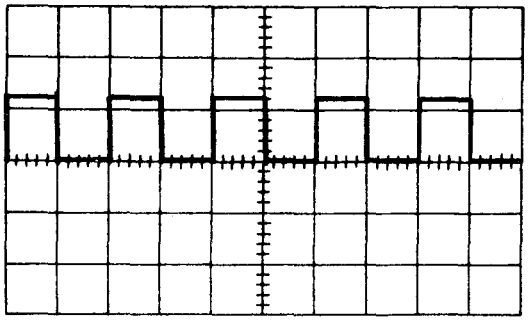
50 µS (S/DIV)

NOTE: ACTUAL DC OFFSET MAY VARY

2 (NO.)

U17-7, 10
U18-7, 10 TP14, TP9

ECL LOGIC LEVELS



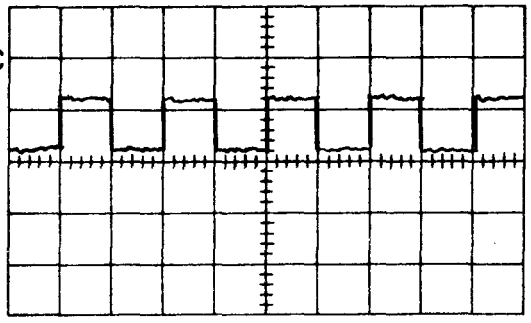
1 (V/DIV)

50 µS (S/DIV)

3 (NO.)

U37-3

ECL LOGIC LEVELS



1 (V/DIV)

0.5 µS (S/DIV)

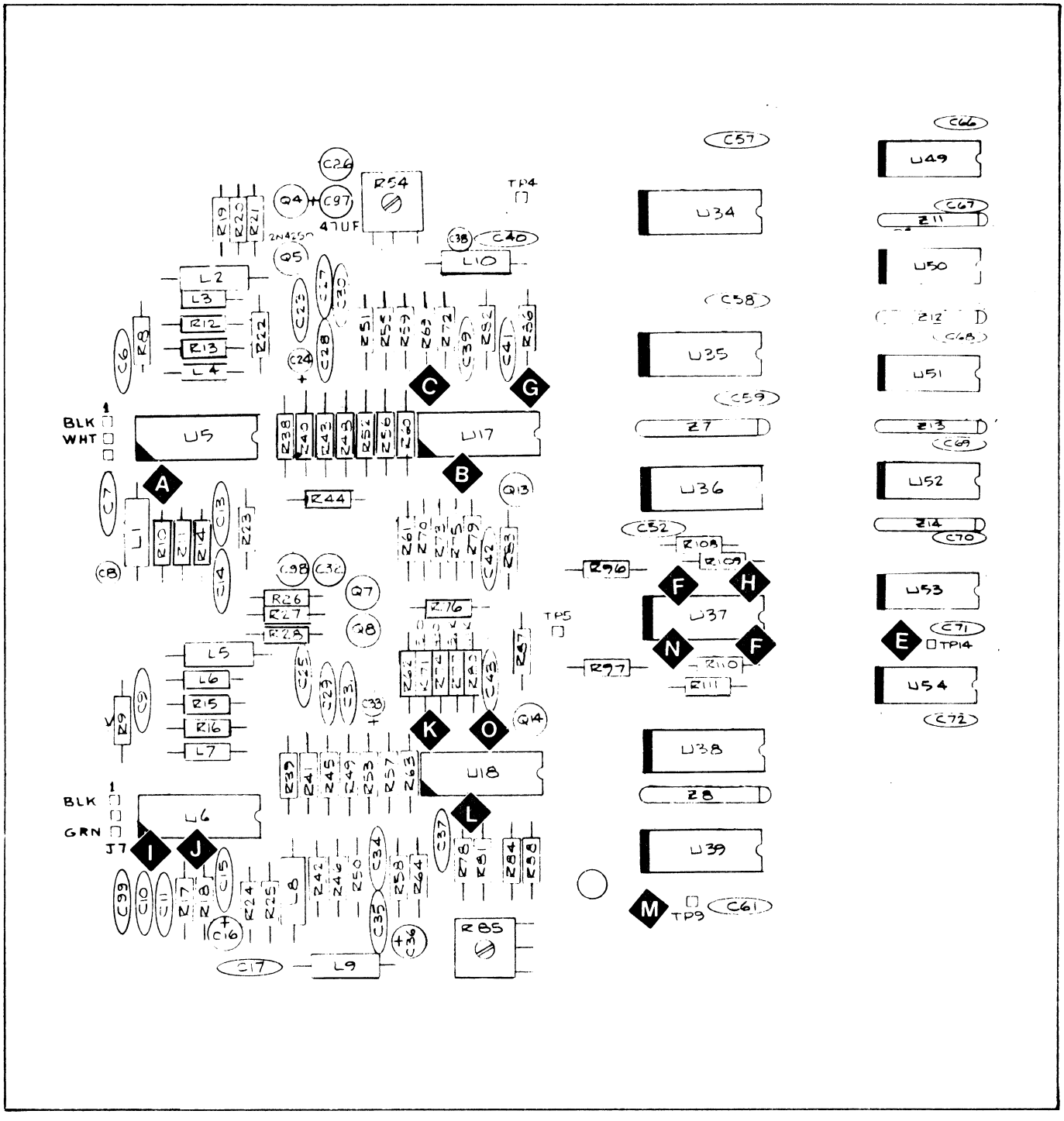


Figure 2.8 - Signal Conditioner Test Point Locations

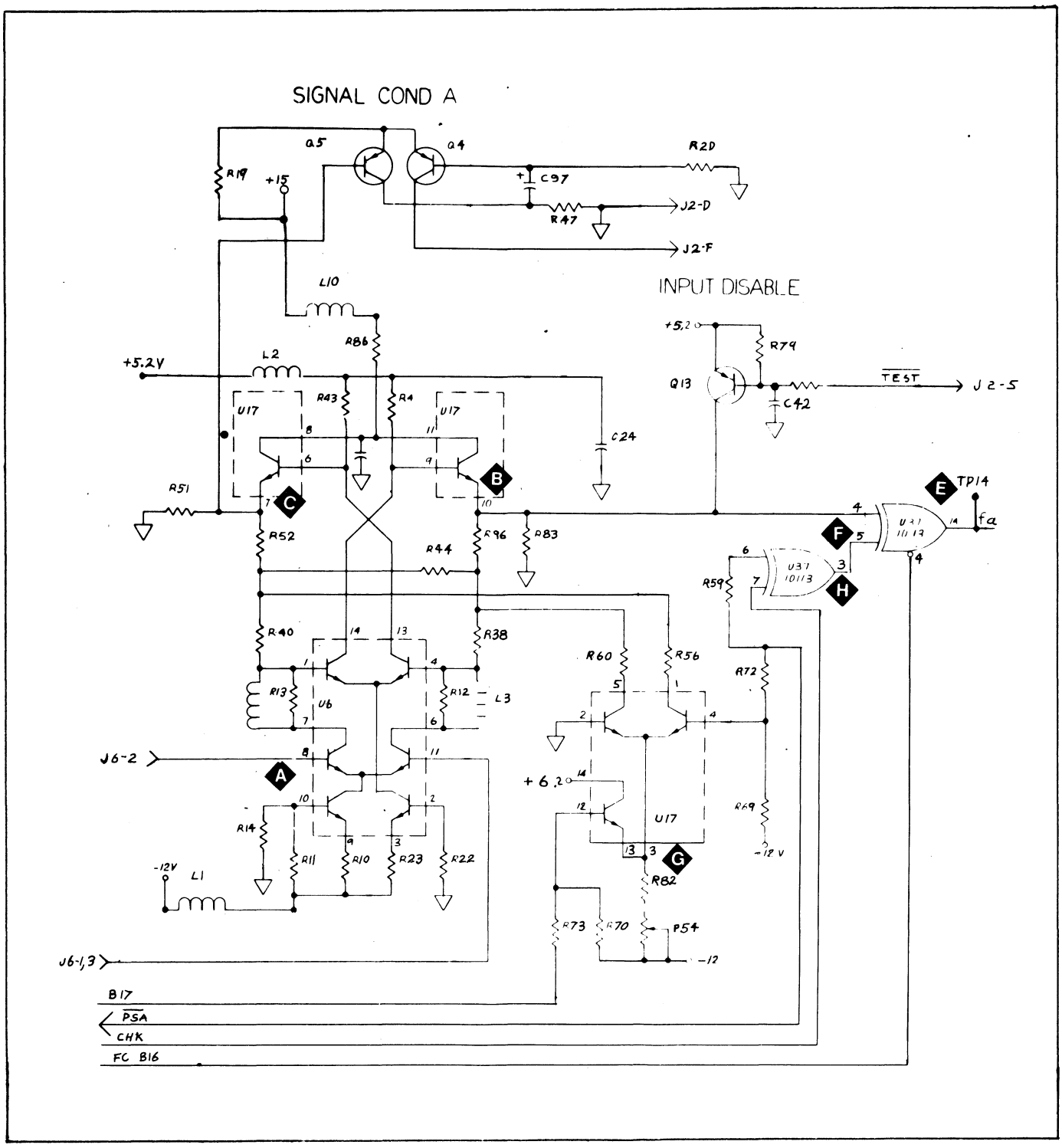


Figure 2.9 - Signal Conditioner A Schematic Test Point Locations

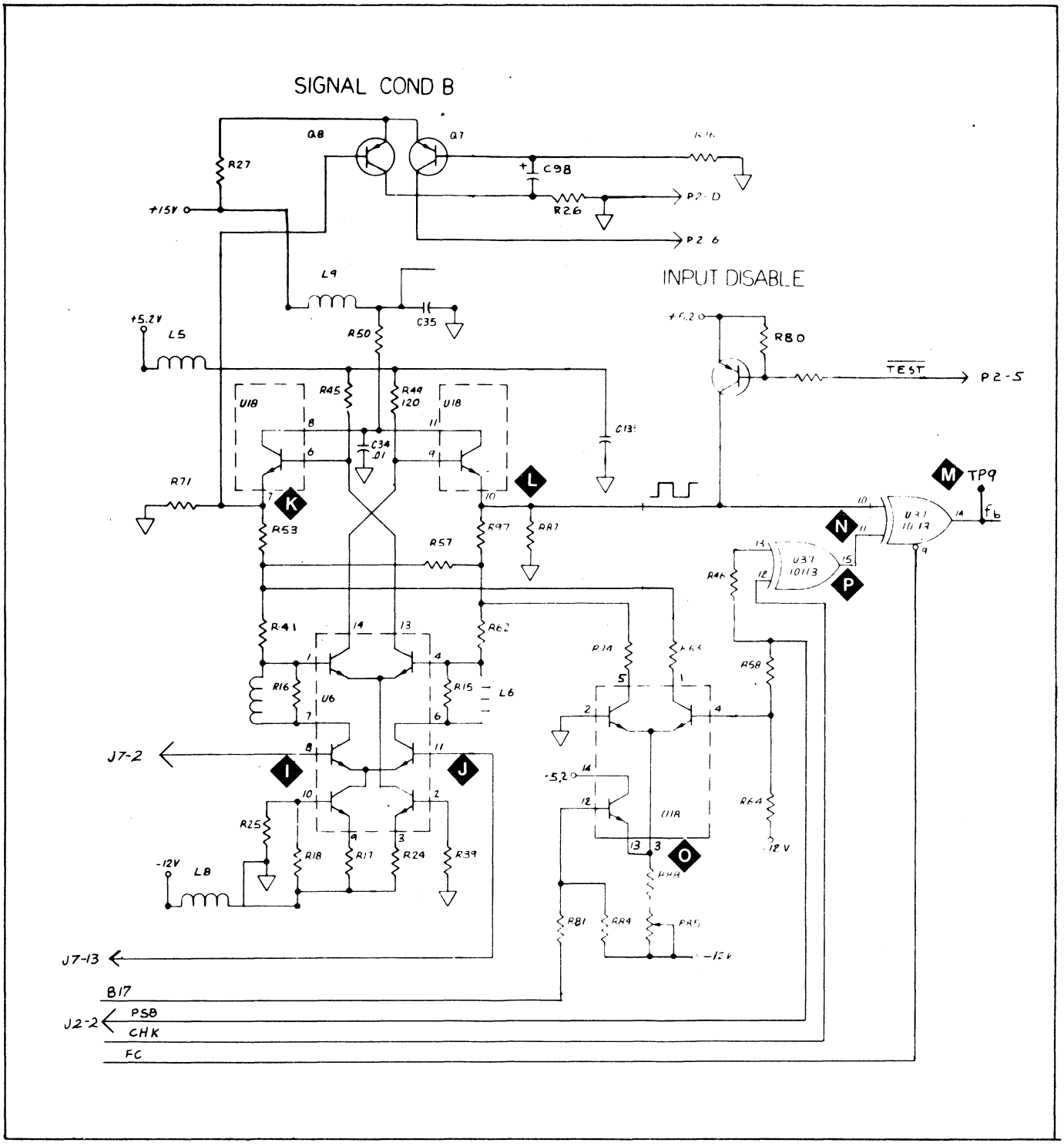


Figure 2.10 - Signal Conditioner B Schematic Test Point Locations

Table 2.6 - Function and Resolution Select Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA	FA	U14-8	1	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: O	FB	U14-6	2	Figures 2.11 & 2.12	⟨ 0.8 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟨ 0.8 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟩ 2.4 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟨ 0.8 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟨ 0.8 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟩ 2.4 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟩ 2.4 V
	RA	U15-8	21	Figures 2.11 & 2.12	⟨ 0.8 V
	RB	U15-6	22	Fgiures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩ 2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟩ 2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟩ 2.4 V
N/RESOLUTION: 1	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟩2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟩2.4 V
N/RESOLUTION: 2	RA	U15-8	21	Figures 2.11 & 2.12	⟨0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨0.8 V
	DPB1	ROM 2-1	24	Figures 2.11 & 2.12	⟨0.8 V
	DPB2	ROM 2-2	25	Figures 2.11 & 2.12	⟩2.4 V
	DPB4	ROM 2-3	25	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM 2-4	27	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM 2-5	28	Figures 2.11 & 2.12	⟩2.4 V
	AB4	ROM 2-6	29	Figures 2.11 & 2.12	⟩2.4 V
N/RESOLUTION: 3	RA	U15-8	21	Figures 2.11 & 2.12	⟩2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨0.8 V
	DPB1	ROM 2-1	24	Figures 2.11 & 2.12	⟩2.4 V
	DPB2	ROM 2-2	25	Figures 2.11 & 2.12	⟩2.4 V
	DPB4	ROM 2-3	26	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM 2-4	27	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM 2-5	28	Figures 2.11 & 2.12	⟩2.4 V
	AB4	ROM 2-6	29	Figures 2.11 & 2.12	⟩2.4 V
N/RESOLUTION: 4	RA	U15-8	21	Figures 2.11 & 2.12	⟨0.8 V
	RB	U15-8	22	Figures 2.11 & 2.12	⟨0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM 2-1	24	Figures 2.11 & 2.12	⟩2.4 V
	DPB2	ROM 2-2	25	Figures 2.11 & 2.12	⟨0.8 V
	DPB4	ROM 2-3	26	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM 2-4	27	Figures 2.11 & 2.12	⟨0.8 V
	AB2	ROM 2-5	28	Figures 2.11 & 2.12	⟩2.4 V
	AB4	ROM 2-6	29	Figures 2.11 & 2.12	⟩2.4 V
N/RESOLUTION: 5	RA	U15-8	21	Figures 2.11 & 2.12	⟩2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	RC	U15-10	23	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM 2-1	24	Figures 2.11 & 2.12	⟨0.8 V
	DPB2	ROM 2-2	25	Figures 2.11 & 2.12	⟩2.4 V
	DPB4	ROM 2-3	26	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM 2-4	27	Figures 2.11 & 2.12	⟨0.8 V
	AB2	ROM 2-5	28	Figures 2.11 & 2.12	⟩2.4 V
	AB4	ROM 2-6	29	Figures 2.11 & 2.12	⟩2.4 V
N/RESOLUTION: 6	RA	U15-8	21	Figures 2.11 & 2.12	⟨0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM 2-1	24	Figures 2.11 & 2.12	⟨0.8 V
	DPB2	ROM 2-2	25	Figures 2.11 & 2.12	⟨0.8 V
	DPB4	ROM 2-3	26	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM 2-4	27	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM 2-5	28	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM 2-6	29	Figures 2.11 & 2.12	⟩2.4 V
N/RESOLUTION: 7	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟩2.4 V
FUNCTION: F C	FA	U14-8	1	Figures 2.11 & 2.12	⟩2.4 V
	FB	U14-6	2	Figures 2.11 & 2.12	⟨ 0.8 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟨ 0.8 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟩ 2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	B3	ROM1-1		Figures 2.11 & 2.12	⟨ 0.8 V
	B5	ROM1-3		Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9		Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4		Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5		Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4		Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9		Figures 2.11 & 2.12	⟩ 2.4 V
	B12	U14-4		Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟩ 2.4 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟩ 2.4 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟩ 2.4 V
FUNCTION: RB	FA	U14-8	1	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 0	FB	U14-6	2	Figures 2.11 & 2.12	⟩ 2.4 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟩ 2.4 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟩ 2.4 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9		Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4		Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟨ 0.8 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	B17	ROM1-6	20	Figures 2.11 & 2.12	〉2.4 V
	RA	U15-8	21	Figures 2.11 & 2.12	〈 0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	〈 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	〈 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	〈 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	〈 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	〈 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	〉2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	〉2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	〉2.4 V
N/RESOLUTION: 1	RA	U15-8	21	Figures 2.11 & 2.12	〉2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	〈 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	〈 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	〉2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	〈 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	〈 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	〈 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	〈 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	〈 0.8 V
N/RESOLUTION: 2	RA	U15-8	21	Figures 2.11 & 2.12	〈 0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	〉2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	〈 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	〈 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	〉2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	〈 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	〈 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	〈 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	〈 0.8 V
N/RESOLUTION: 3	RA	U15-8	21	Figures 2.11 & 2.12	〉2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	〉2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	〈 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	〉2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 4	RA	U15-8	21	Figures 2.11 & 2.12	⟨ 0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟩ 2.4 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨ 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 5	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟩ 2.4 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨ 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 6	RA	U15-8	21	Figures 2.11 & 2.12	⟨0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩ 2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟨0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟩ 2.4 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
N/RESOLUTION: 7	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩ 2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟩ 2.4 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨ 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
FUNCTION: RC	FA	U14-8	1	Figures 2.11 & 2.12	⟩ 2.4 V
	FB	U14-6	2	Figures 2.11 & 2.12	⟩ 2.4 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟩ 2.4 V
	B2	U11-7	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟩ 2.4 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 5.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟩ 2.4 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟨0.8 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟩ 2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: P	FA	U14-8	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
N/RESOLUTION: O	FB	U14-6	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	FC	U14-10	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	FC	U14-4	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B2	U11-7	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B5	ROM1-3	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	B7	ROM1-4	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U4-6	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15-12	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	RA	U15-8	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	RB	U15-6	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM 2-1	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM 2-2	[illegible]	Figures 5.11 & 5.12	⟨ 0.8 V
	DPB4	ROM 2-3	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM 2-4	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM 2-5	[illegible]	Figures 2.11 & 2.12	⟩ 2.4 V
	AB4	ROM 2-6	[illegible]	Figures 2.11 & 2.12	⟨ 0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
N/RESOLUTION: 1	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟩ 2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 2	RA	U15-8	21	Figures 2.11 & 2.12	⟨ 0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩ 2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩ 2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟩ 2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 3	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩ 2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩ 2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟩ 2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 4	RA	U15-8	21	Figures 2.11 & 2.12	⟨ 0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	DPB 4	ROM 2 - 3	26	Figures 2.11 & 2.12	〉2.4 V
	AB 1	ROM 2 - 4	27	Figures 2.11 & 2.12	〈0.8 V
	AB 2	ROM 2 - 5	28	Figures 2.11 & 2.12	〈0.8 V
	AB 4	ROM 2 - 6	29	Figures 2.11 & 2.12	〉2.4 V
N/RESOLUTION: 5	R A	U15 – 8	21	Figures 2.11 & 2.12	〉2.4 V
	R B	U15 – 6	22	Figures 2.11 & 2.12	〈0.8 V
	R C	U15 – 10	23	Figures 2.11 & 2.12	〉2.4 V
	DPB 1	ROM 2 - 1	24	Figures 2.11 & 2.12	〈0.8 V
	DPB 2	ROM 2 - 2	25	Figures 2.11 & 2.12	〉2.4 V
	DPB 4	ROM 2 - 3	26	Figures 2.11 & 2.12	〈0.8 V
	AB 1	ROM 2 - 4	27	Figures 2.11 & 2.12	〈0.8 V
	AB 2	ROM 2 - 5	28	Figures 2.11 & 2.12	〈0.8 V
	AB 4	ROM 2 - 6	29	Figures 2.11 & 2.12	〉2.4 V
N/RESOLUTION: 6	R A	U15 – 8	21	Figures 2.11 & 2.12	〉2.4 V
	R B	U15 – 6	22	Figures 2.11 & 2.12	〉2.4 V
	R C	U15 – 10	23	Figures 2.11 & 2.12	〈0.8 V
	DPB 1	ROM 2 - 1	24	Figures 2.11 & 2.12	〉2.4 V
	DPB 2	ROM 2 - 2	25	Figures 2.11 & 2.12	〈0.8 V
	DPB 4	ROM 2 - 3	26	Figures 2.11 & 2.12	〈0.8 V
	AB 1	ROM 2 - 4	27	Figures 2.11 & 2.12	〈0.8 V
	AB 2	ROM 2 - 5	28	Figures 2.11 & 2.12	〈0.8 V
	AB 4	ROM 2 - 6	29	Figures 2.11 & 2.12	〉2.4 V
N/RESOLUTION: 7	R A	U15 – 8	21	Figures 2.11 & 2.12	〉2.4 V
	R B	U15 – 6	22	Figures 2.11 & 2.12	〉2.4 V
	R C	U15 – 10	23	Figures 2.11 & 2.12	〉2.4 V
	DPB 1	ROM 2 - 1	24	Figures 2.11 & 2.12	〈0.8 V
	DPB 2	ROM 2 - 2	25	Figures 2.11 & 2.12	〈0.8 V
	DPB 4	ROM 2 - 3	26	Figures 2.11 & 2.12	〈0.8 V
	AB 1	ROM 2 - 4	27	Figures 2.11 & 2.12	〈0.8 V
	AB 2	ROM 2 - 5	28	Figures 2.11 & 2.12	〈0.8 V
	AB 4	ROM 2 - 6	29	Figures 2.11 & 2.12	〉2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: T I	F A	U14 – 8	1	Figures 2.11 & 2.12	⟩ 2.4 V
	F B	U14 – 6	2	Figures 2.11 & 2.12	⟨ 0.8 V
	F C	U14 – 10	3	Figures 2.11 & 2.12	⟩ 2.4 V
	F D	U14 – 4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	B Ø	ROM 1 - 2	5	Figures 2.11 & 2.12	⟨ 0.8 V
	B 1	ROM 2 - 7	6	Figures 2.11 & 2.12	⟨ 0.8 V
	B 2	U11 – 1	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B 3	ROM 1 - 1	8	Figures 2.11 & 2.12	⟨ 0.8 V
	B 5	ROM 1 - 3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B 6	ROM 2 - 9	10	Figures 2.11 & 2.12	⟩ 2.4 V
	B 7	ROM 1 - 4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B 8	ROM 1 - 5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B 9	U23 – 4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10 – 8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM 1 - 9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14 – 4	16	Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U 4 – 6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM 1 - 7	18	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15 – 12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM 1 - 6	20	Figures 2.11 & 2.12	⟨ 0.8 V
	AB 1	ROM 2 - 4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB 2	ROM 2 - 5	28	Figures 2.11 & 2.12	⟩ 2.4 V
	AB 4	ROM 2 - 6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 2	R A	U15 – 8	21	Figures 2.11 & 2.12	⟨ 0.8 V
	R B	U15 – 6	22	Figures 2.11 & 2.12	⟩ 2.4 V
	R C	U15 – 10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB 1	ROM 2 - 1	24	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB 2	ROM 2 - 2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DBB 4	ROM 2 - 3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB 1	ROM 2 - 4	27	Figures 2.11 & 2.12	⟩ 2.4 V
	AB 2	ROM 2 - 5	28	Figures 2.11 & 2.12	⟨ 0.8 V
	AB 4	ROM 2 - 6	29	Figures 2.11 & 2.12	⟨ 0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
N/RESOLUTION: 3	RA	U15-8	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	RB	U15-6	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	RC	U15-10	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	DPB1	ROM2-1	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB2	ROM2-2	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	DPB4	ROM2-3	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM2-4	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM2-5	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM2-6	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
N/RESOLUTION: 4	RA	U15-8	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	RB	U15-6	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	RC	U15-10	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM2-1	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	DPB2	ROM2-2	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB4	ROM2-3	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM2-4	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM2-5	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM2-6	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
N/RESOLUTION: 5	RA	U15-8	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	RB	U15-6	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	RC	U15-10	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM2-1	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB2	ROM2-2	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB 4	ROM2-3	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	AB1	ROM2-4	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	AB2	ROM2-5	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	AB4	ROM2-6	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
N/RESOLUTION: 6	RA	U15-8	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	RB	U15-6	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	RC	U15-10	[illegible]	Figures 2.11 & 2.12	⟩2.4 V
	DPB1	ROM2-1	[illegible]	Figures 2.11 & 2.12	⟨0.8 V
	DPB2	ROM2-2	[illegible]	Figures 2.11 & 2.12	⟨0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟩ 2.4 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩ 2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨ 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 7	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟩ 2.4 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟩ 2.4 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟩ 2.4 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟨ 0.8 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
FUNCTION: PA	FA	U14-8	1	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: Ø	FB	U14-6	2	Figures 2.11 & 2.12	⟩ 2.4 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟩ 2.4 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟩ 2.4 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟩ 2.4 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟩ 2.4 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟩ 2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	RA	U15-8	21	Figures 2.11 & 2.12	⟨ 0.8 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
	AB1	ROM2-4	27	Figures 2.11 & 2.12	⟨ 0.8 V
	AB2	ROM2-5	28	Figures 2.11 & 2.12	⟩ 2.4 V
	AB4	ROM2-6	29	Figures 2.11 & 2.12	⟨ 0.8 V
N/RESOLUTION: 1	RA	U15-8	21	Figures 2.11 & 2.12	⟩ 2.4 V
	RB	U15-6	22	Figures 2.11 & 2.12	⟨ 0.8 V
	RC	U15-10	23	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB1	ROM2-1	24	Figures 2.11 & 2.12	⟨ 0.8 V
	DPB2	ROM2-2	25	Figures 2.11 & 2.12	⟩ 2.4 V
	DPB4	ROM2-3	26	Figures 2.11 & 2.12	⟨ 0.8 V
FUNCTION: TIA	FA	U14-8	1	Figures 2.11 & 2.12	⟩ 2.4 V
	FB	U14-6	2	Figures 2.11 & 2.12	⟩ 2.4 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟩ 2.4 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟨ 0.8 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟩ 2.4 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟨ 0.8 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟨ 0.8 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟨ 0.8 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟩ 2.4 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟨ 0.8 V
FUNCTION: FB	FA	U14-8	1	Figures 2.11 & 2.12	⟨ 0.8 V
	FB	U14-6	2	Figures 2.11 & 2.12	⟨ 0.8 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟩ 2.4 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟩ 2.4 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟨ 0.8 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟩ 2.4 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟨ 0.8 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟨ 0.8 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟨ 0.8 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟩ 2.4 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟩ 2.4 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟩ 2.4 V
FUNCTION: C/A→ B	FA	U14-8	1	Figures 2.11 & 2.12	⟩ 2.4 V
	FB	U14-6	2	Figures 2.11 & 2.12	⟨ 0.8 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟩ 2.4 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟨ 0.8 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟨ 0.8 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟩ 2.4 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟩ 2.4 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V

Table 2.6 - Function and Resolution Select Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟩ 2.4 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟩ 2.4 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟩ 2.4 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟩ 2.4 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟨ 0.8 V
FUNCTION: TOT	FA	U14-8	1	Figures 2.11 & 2.12	⟨ 0.8 V
	FB	U14-6	2	Figures 2.11 & 2.12	⟩ 2.4 V
	FC	U14-10	3	Figures 2.11 & 2.12	⟨ 0.8 V
	FD	U14-4	4	Figures 2.11 & 2.12	⟩ 2.4 V
	BØ	ROM1-2	5	Figures 2.11 & 2.12	⟨ 0.8 V
	B1	ROM2-7	6	Figures 2.11 & 2.12	⟩ 2.4 V
	B2	U11-1	7	Figures 2.11 & 2.12	⟨ 0.8 V
	B3	ROM1-1	8	Figures 2.11 & 2.12	⟩ 2.4 V
	B5	ROM1-3	9	Figures 2.11 & 2.12	⟨ 0.8 V
	B6	ROM2-9	10	Figures 2.11 & 2.12	⟨ 0.8 V
	B7	ROM1-4	11	Figures 2.11 & 2.12	⟨ 0.8 V
	B8	ROM1-5	12	Figures 2.11 & 2.12	⟩ 2.4 V
	B9	U23-4	13	Figures 2.11 & 2.12	⟩ 2.4 V
	B10	U10-8	14	Figures 2.11 & 2.12	⟩ 2.4 V
	B11	ROM1-9	15	Figures 2.11 & 2.12	⟨ 0.8 V
	B12	U14-4	16	Figures 2.11 & 2.12	⟩ 2.4 V
	B14	U4-6	17	Figures 2.11 & 2.12	⟨ 0.8 V
	B15	ROM1-7	18	Figures 2.11 & 2.12	⟨ 0.8 V
	B16	U15-12	19	Figures 2.11 & 2.12	⟨ 0.8 V
	B17	ROM1-6	20	Figures 2.11 & 2.12	⟩ 2.4 V

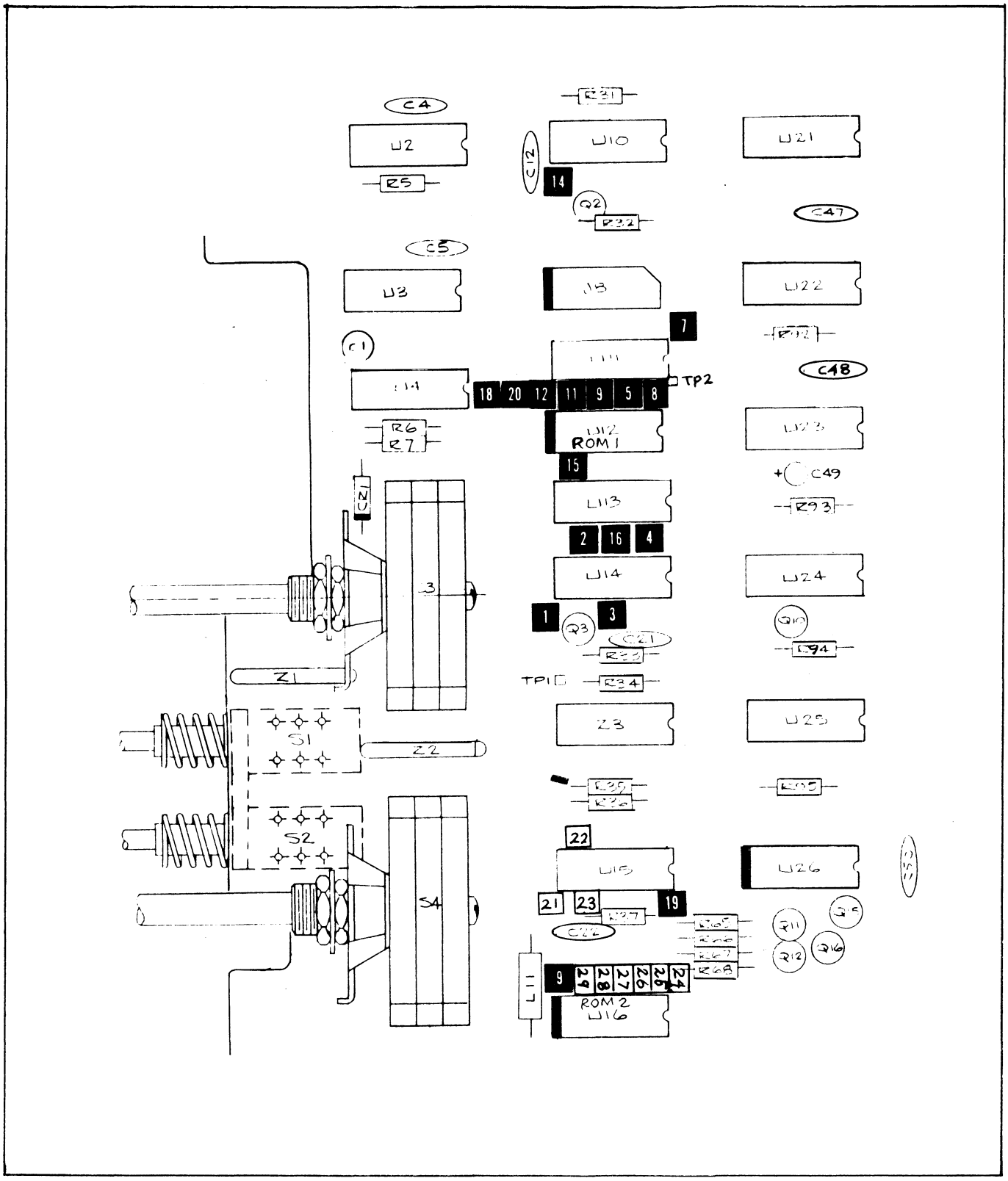


Figure 2.11 - Function and Resolution Test Point Locations

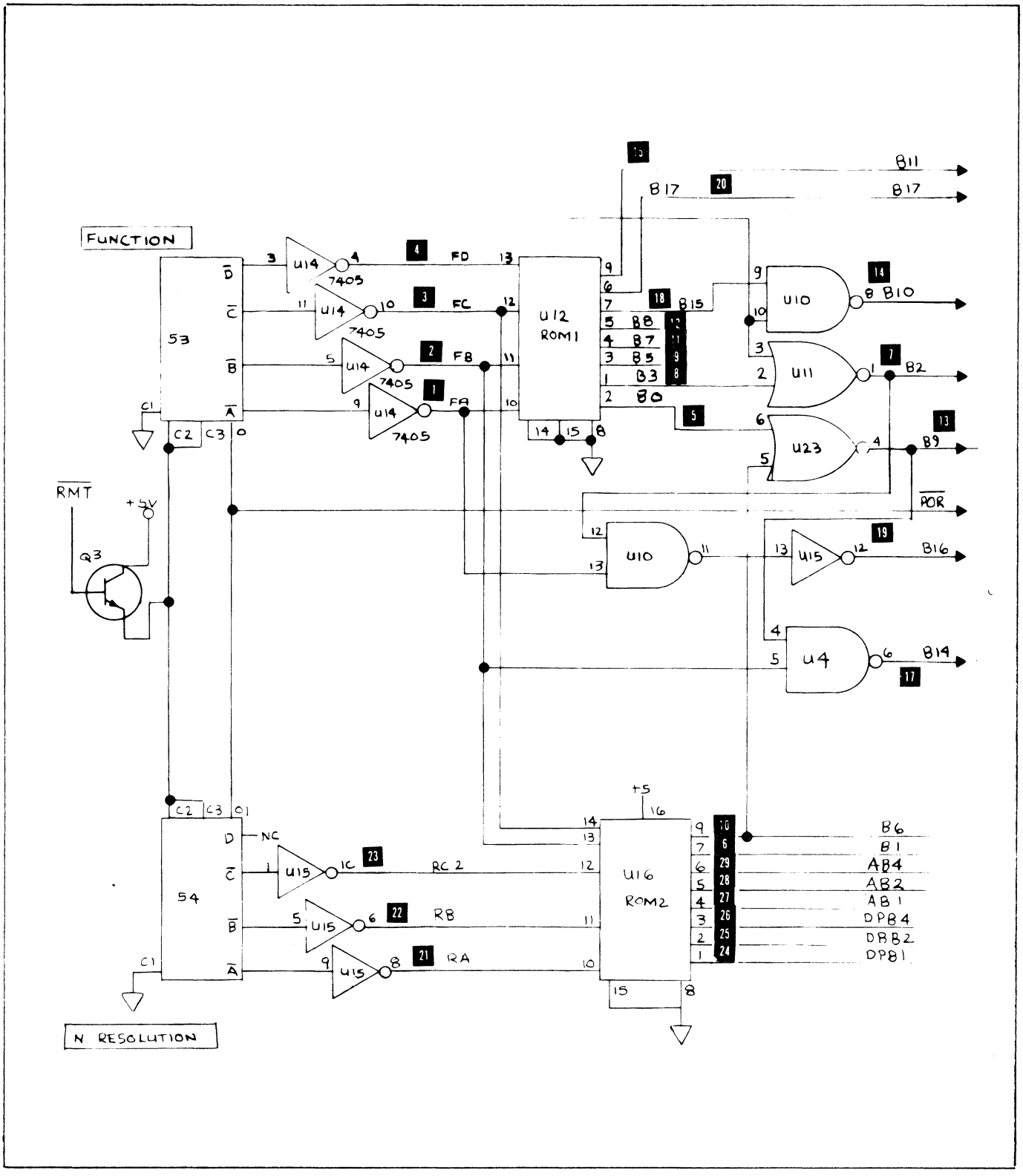


Figure 2.12 - Function and Resolution Schematic Test Point Locations

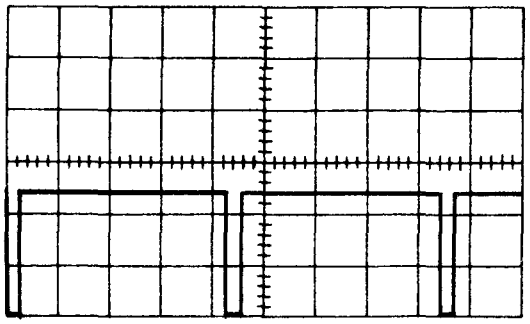
Table 2.7 - Measurement Cycle Timing (Reset Logic) Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA N/RESOLUTION: O TEST/COM/SEP: Test		U27-2	A	Figures 2.13 & 2.14	Waveform 1
	CLEAR	TP6	B	Figures 2.13 & 2.14	Waveform 2
Press RESET Switch.		TP6	1	Figures 2.13 & 2.14	+ 4.2 V
		U3-11	C	Figures 2.13 & 2.14	Waveform 2
		U3-13	D	Figures 2.13 & 2.14	Waveform 3
	$\overline{\text{UPDATE}}$	TP10	E	Figures 2.13 & 2.14	Waveform 4
	$\overline{\text{RMT}}$	J9-15	2	Figures 2.13 & 2.14	⟩ 2.4 V
		J9-8	3	Figures 2.13 & 2.14	⟩ 2.4 V
		J9-10	4	Figures 2.13 & 2.13	⟩ 2.4 V
		J9-2	5	Figures 2.13 & 2.14	⟩ 2.4 V
		J9-11	6	Figures 2.13 & 2.14	⟩ 2.4 V
		J8-14	F	Figures 2.13 & 2.14	⟨ 0.8 V for Model 9514. High frequency noise and dc level below 1.5 V for Model 9510.
		J8-1	G	Figures 2.13 & 2.14	Oscillation with a 10 KHZ period in Model 9510. Oscillation of 26 KHZ period Model 9514.

Waveforms for Table 2.7

1 (NO.)

U27-2

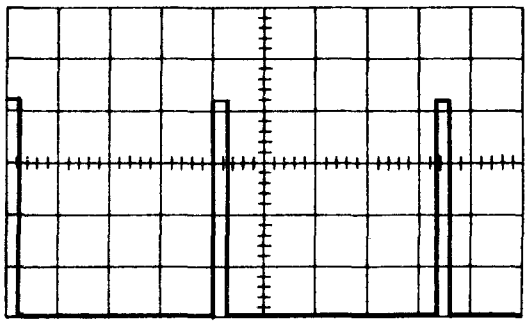


1 (V/DIV)

1 mS (S/DIV)

2 (NO.)

TP6
CLEAR

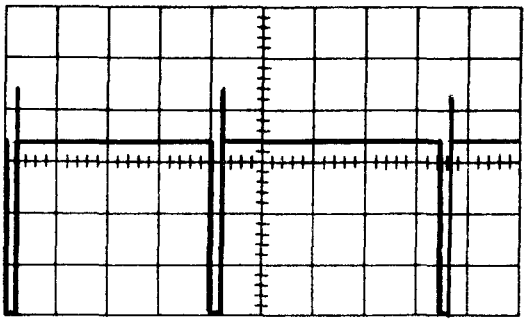


1 (V/DIV)

1 mS (S/DIV)

3 (NO.)

U3-13

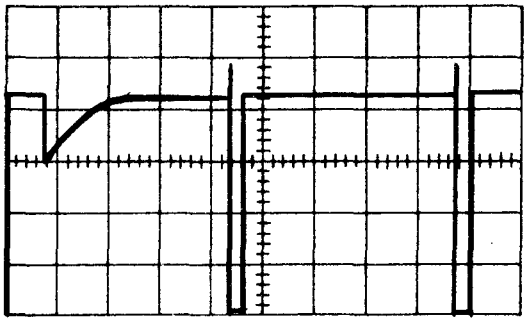


1 (V/DIV)

1 mS (S/DIV)

4 (NO.)

TP10



1 (V/DIV)

1 mS (S/DIV)

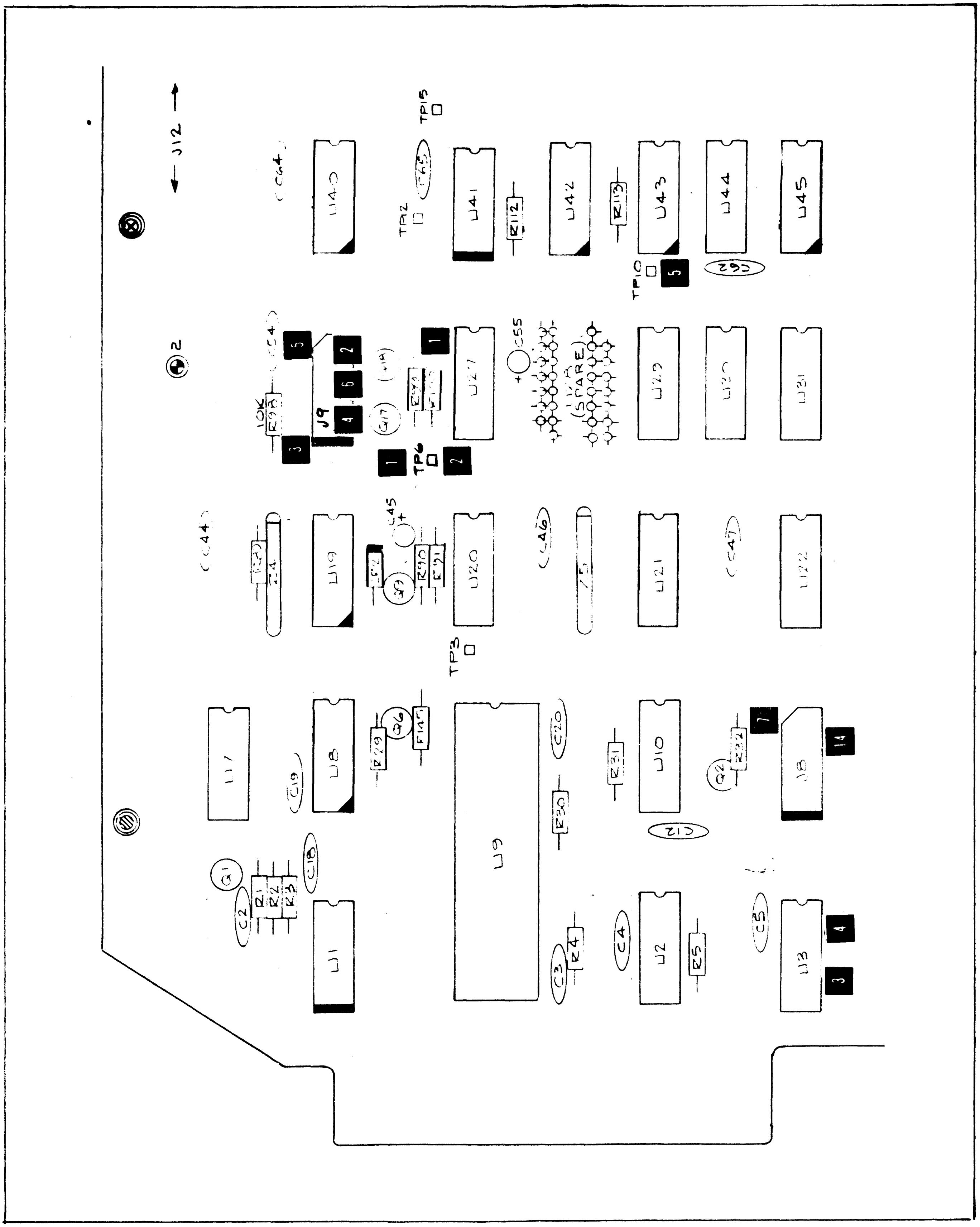


Figure 2.13 - Measurement Cycle Timing (Reset Logic) Test Point Locations

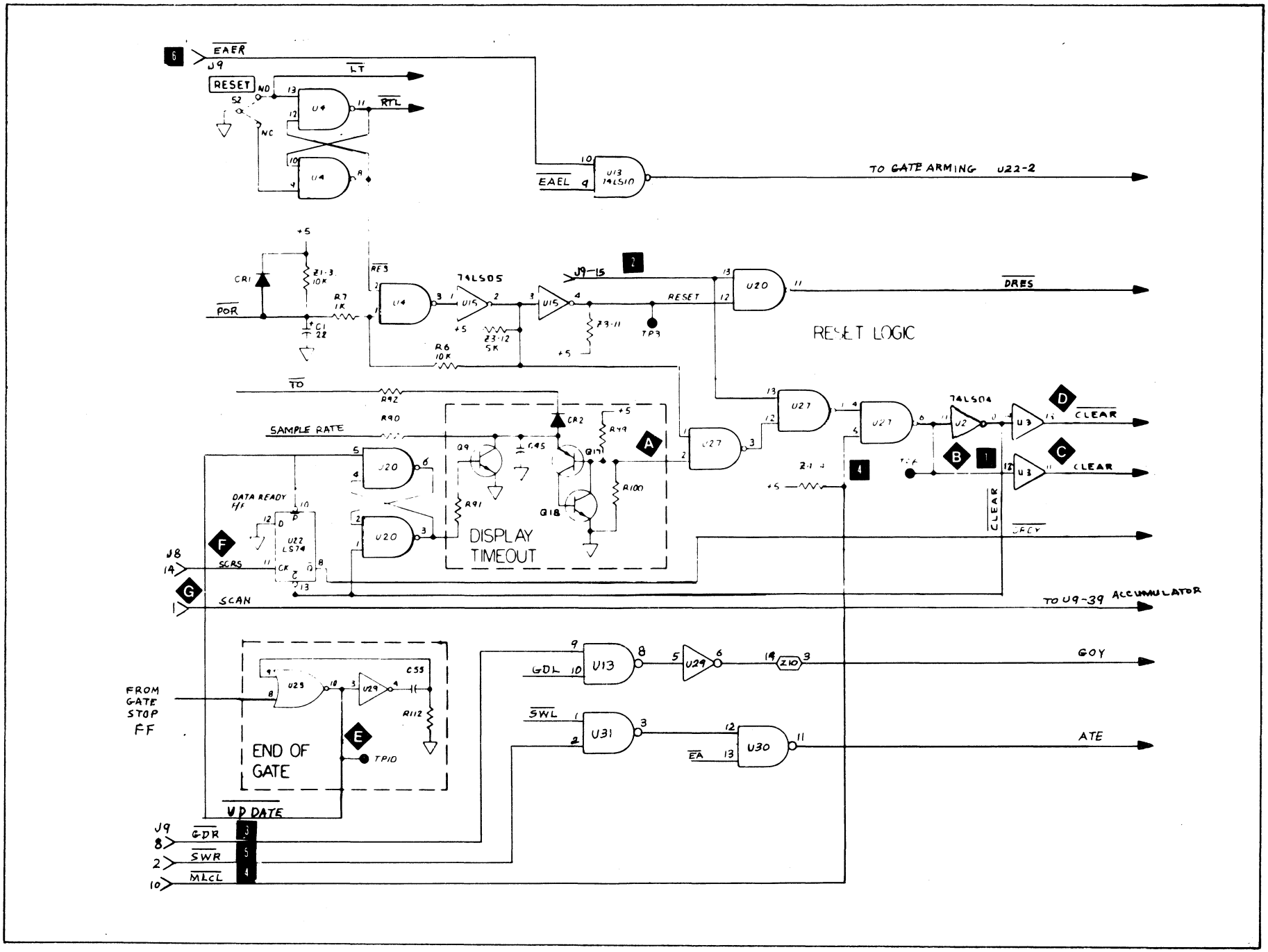


Figure 2.14 - Measurement Cycle Timing (Reset Logic) Schematic Test Point Locations

Table 2.8 - Timebase Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA N/RESP LUTION: 7 TEST/COM/SEP: Test		U45-1	A	Figures 2.15 & 2.17	Waveform 1
		U44-1	B	Figures 2.15 & 2.17	Waveform 2
		U44-4	C	Figures 2.15 & 2.17	Waveform 2
		U44-3	D	Figures 2.15 & 2.17	Waveform 2
FUNCTION: P		U33-11	E	Figures 2.15 & 2.17	Waveform 1
		U48-6	F	Figures 2.15 & 2.17	Waveform 1
		U41-4	G	Figures 2.15 & 2.17	Waveform 1
FUNCTION: PA		U44-11	H	Figures 2.15 & 2.17	Waveform 1
		U44-6	I	Figures 2.15 & 2.17	Waveform 1
		U41-4	G	Figures 2.15 & 2.17	Waveform 1
FUNCTION: FA					80% duty-cycle pulse Period
		U41-4	G	Figures 2.15 & 2.17	1 μs
		U41-4	J	Figures 2.15 & 2.17	10 μs
		U41-2	K	Figures 2.15 & 2.17	100 μs
		U41-1	L	Figures 2.15 & 2.17	1 ms
		U41-15	M	Figures 2.15 & 2.17	10 ms
		U41-14	N	Figures 2.15 & 2.17	100 ms
		U41-13	O	Figures 2.15 & 2.17	1 sec
		U41-12	P	Figures 2.15 & 2.17	10 sec
FUNCTION: TOT		TP-12		Figures 2.15 & 2.17	
N/RESOLUTION					Period
0				Figures 2.15 & 2.17	0.1 μs
1				Figures 2.15 & 2.17	1 μs
2				Figures 2.15 & 2.17	10 μs
3				Figures 2.15 & 2.17	100 μs
4				Figures 2.15 & 2.17	1 ms
5				Figures 2.15 & 2.17	10 ms
6				Figures 2.15 & 2.17	100 ms
7				Figures 2.15 & 2.17	1 sec

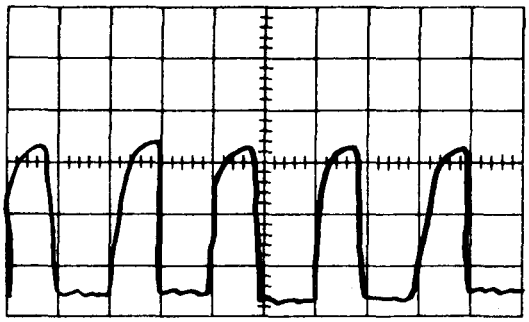
Table 2.8 - Timebase Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA N/RESOLUTION: 0	GATE	U35-15	Q	Figures 2.15 & 2.17	Waveform 3
N/RESOLUTION: 3		U35-15	Q	Figures 2.15 & 2.17	Waveform 4
REF INT/EXT: EXT (Rear Panel) Apply a 1 VRMS 10 MHz sinewave to REF rear panel connector.		U63-9	R	Figures 2.16 & 2.18	Waveform 5
		U63-8	S	Figures 2.16 & 2.18	Waveform 6
		U63-10	T	Figures 2.16 & 2.18	Waveform 7
		U63-13	U	Figures 2.16 & 2.18	Waveform 8

Waveforms for Table 2.8

U45-1

1 (NO.)

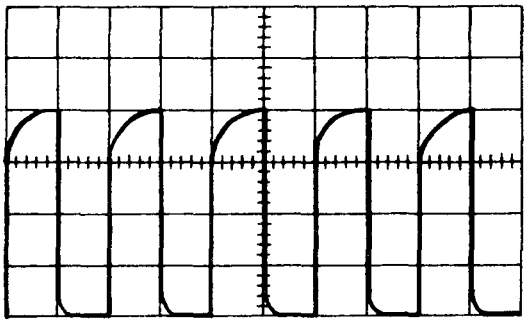


1 (V/DIV)

0.05 µS (S/DIV)

U44-1

2 (NO.)



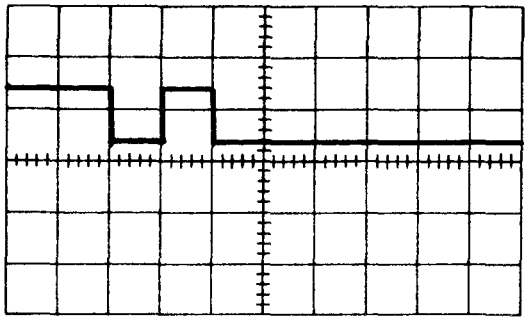
1 (V/DIV)

0.5 µS (S/DIV)

U35-15

3 (NO.)

GATE TIME



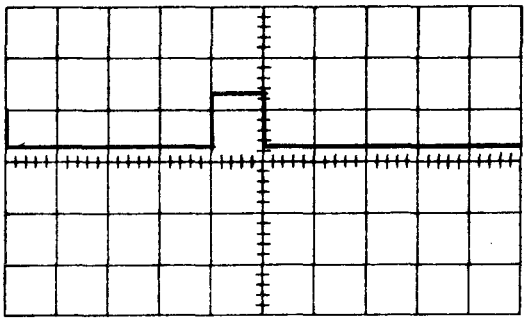
1 (V/DIV)

0.5 µS (S/DIV)

EXT SYNC AT TP6 – SLOPE

U35-15

4 (NO.)



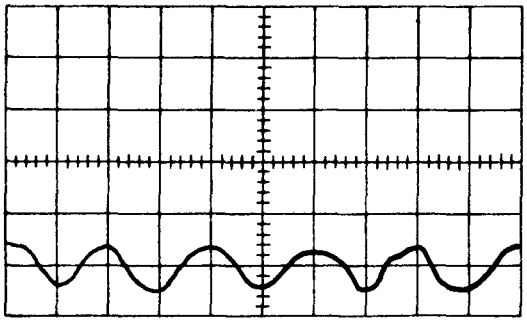
1 (V/DIV)

0.2 mS (S/DIV)

Waveforms for Table 2.8 continued

U63-9

5 (NO.)

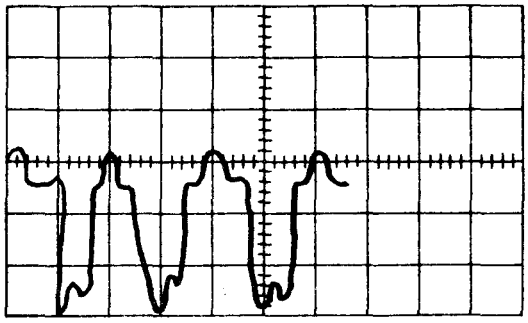


1 (V/DIV)

0.05 μS (S/DIV)

U63-8

6 (NO.)

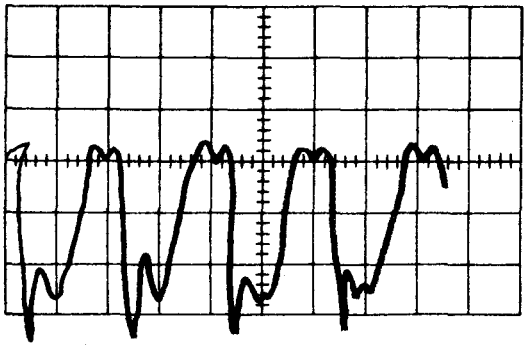


1 (V/DIV)

0.05 μS (S/DIV)

U63-10

7 (NO.)

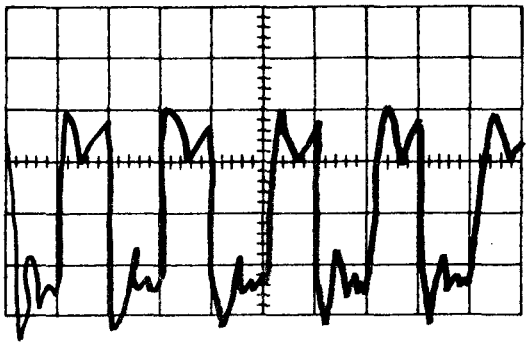


1 (V/DIV)

0.05 μS (S/DIV)

U63-13

8 (NO.)



1 (V/DIV)

0.05 μS (S/DIV)

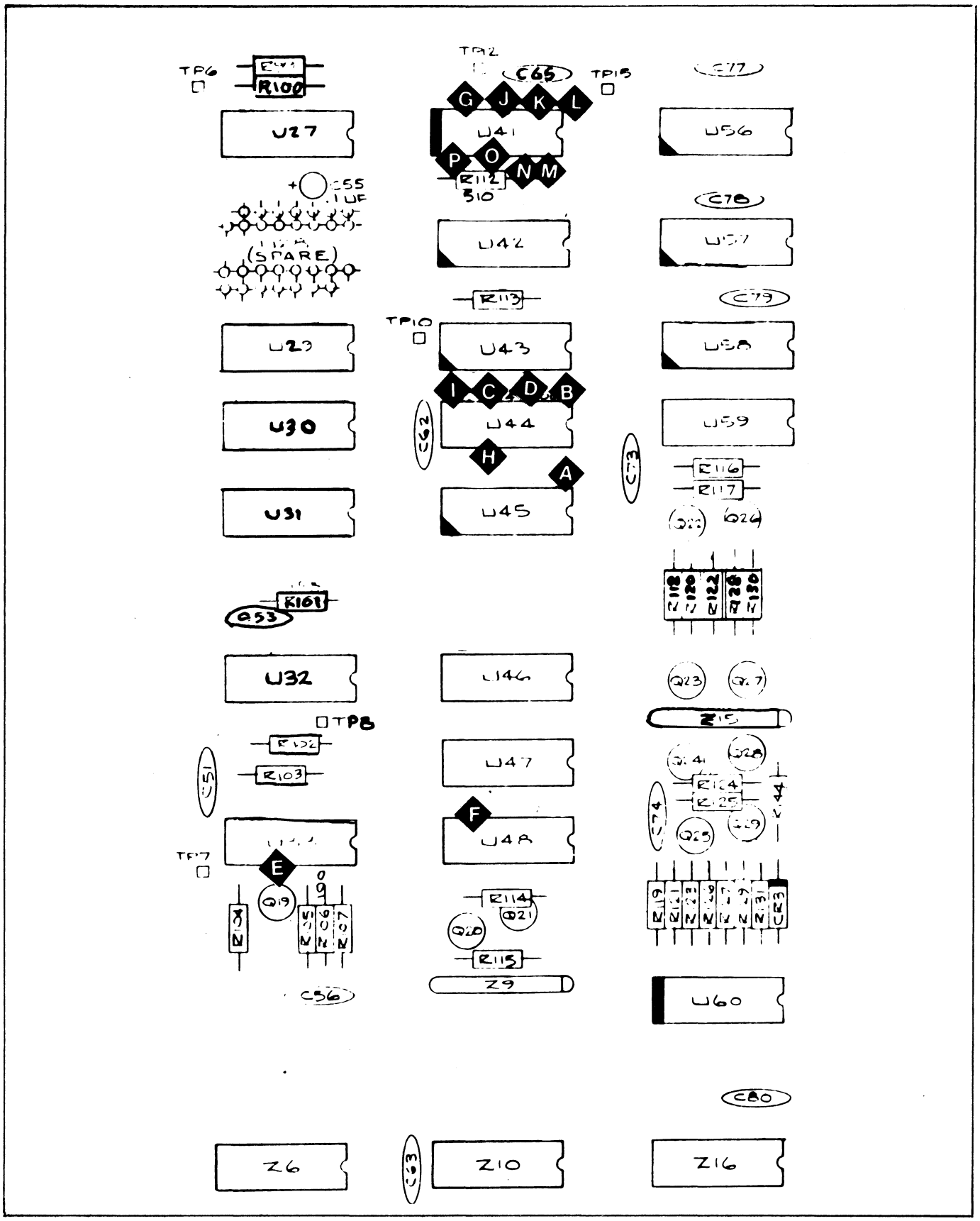


Figure 2.15 - Timebase Test Point Locations

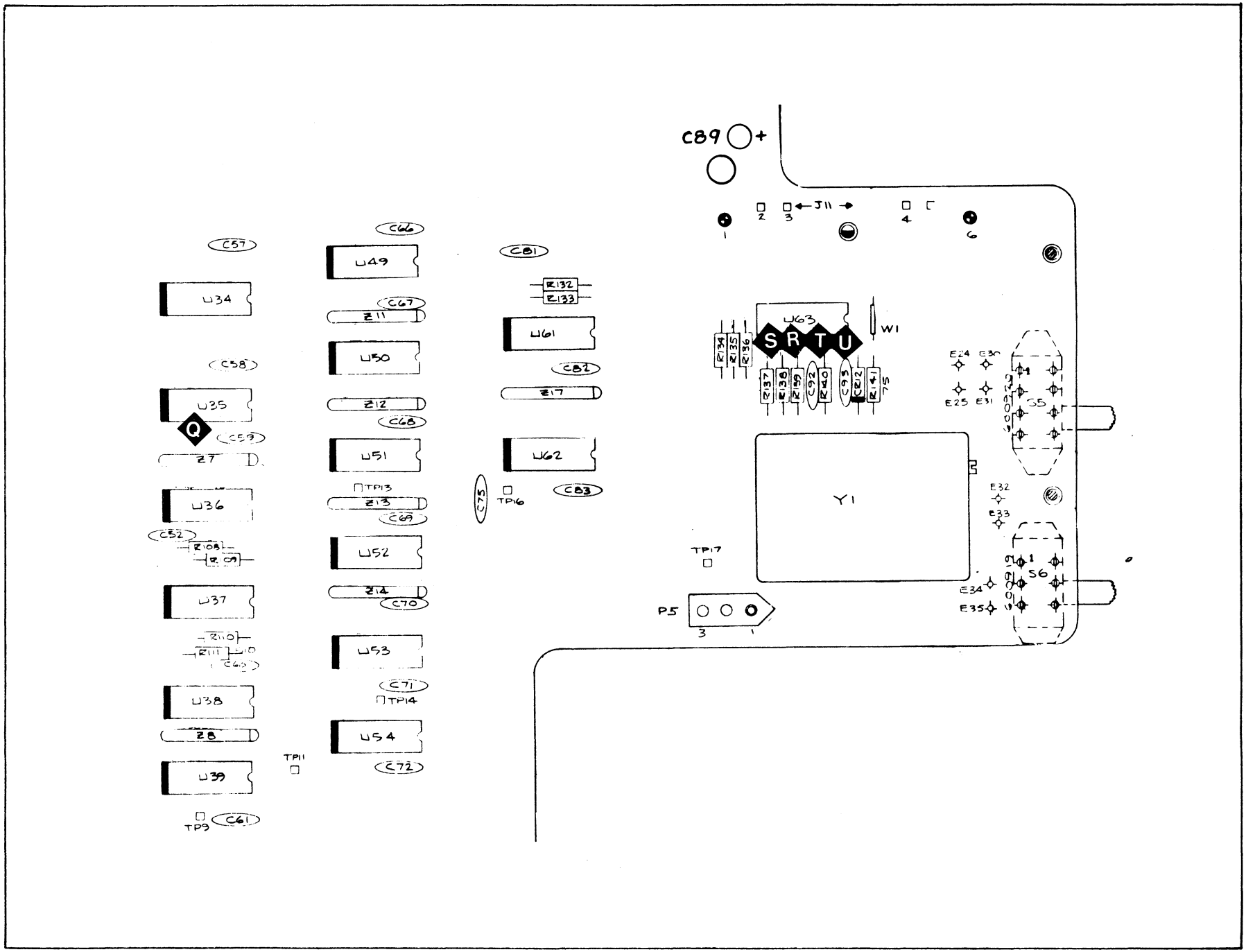


Figure 2.16 - Timebase and Reference Signal Conditioner Test Point Locations

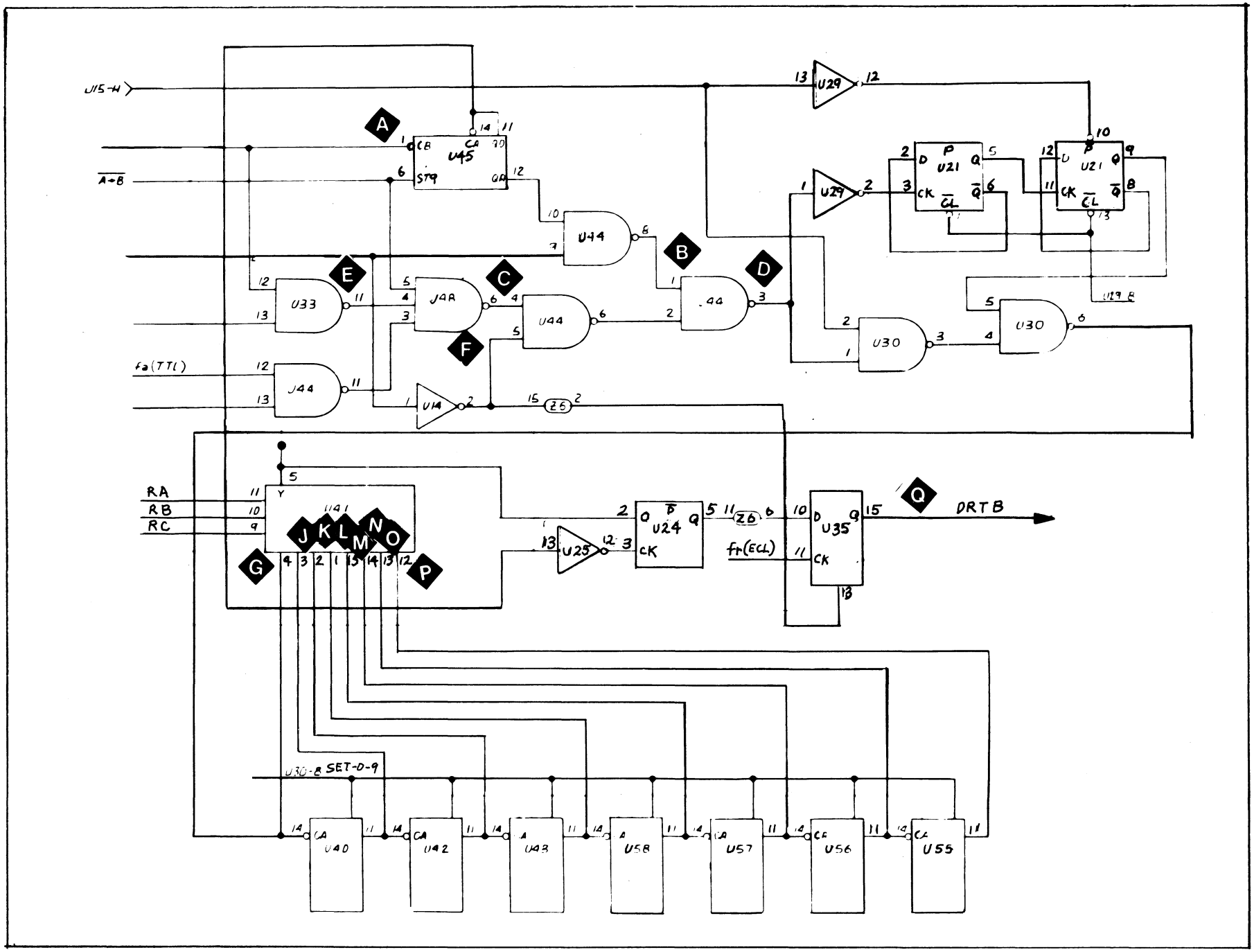


Figure 2.17 - Timebase Schematic Test Point Locations

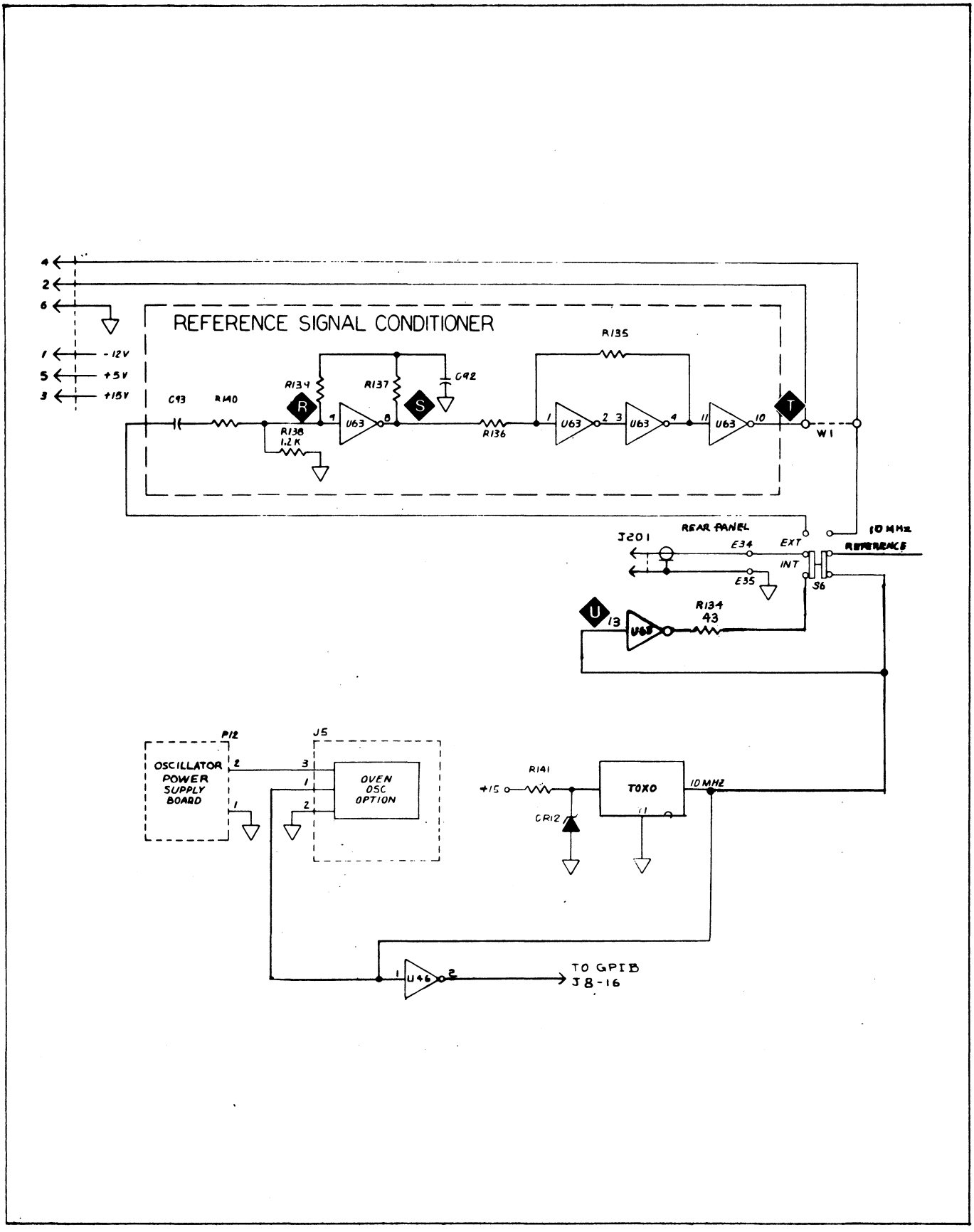


Figure 2.18 - Timebase and Reference Signal Conditioner Schematic Test Point Locations

Table 2.9 - Measurement Gate and Gate Control Performance Test

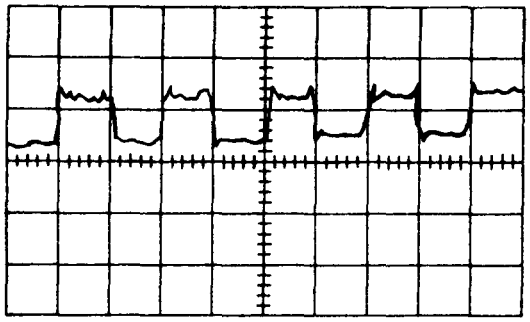
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: P		U62-14	A	Figures 2.19 & 2.20	Waveform 1
N/RESOLUTION: 0		U62-3	B	Figures 2.19 & 2.20	Waveform 1
TEST/COM/SEP: TEST					
FUNCTION: TIA		U62-3	B	Figures 2.19 & 2.20	Waveform 2
N/RESOLUTION: 1		U62-14	A	Figures 2.19 & 2.20	Waveform 2
TEST/COM/SEP: COM					
Apply a 1 V RMS, 100 KHz sinewave to INPUT A.					
FUNCTION: TI		U62-3	B	Figures 2.19 & 2.20	Waveform 3
TEST/COM/SEP: COM		U62-14	A	Figures 2.19 & 2.20	Waveform 3
FUNCTION: TOT		U62-3	B	Figures 2.19 & 2.20	3.4 Volt
Press the START/STOP switch.		U62-14	A	Figures 2.19 & 2.20	4.2 Volts Returns to 3.4 when START is released.
FUNCTION: FA		U62-3	B	Figures 2.19 & 2.20	Waveform 4
TEST/COM/SEP: TEST		U62-14	A	Figures 2.19 & 2.20	Waveform 4
N/RESOLUTION: 0					
FUNCTION: FA					
TEST/COM/SEP: TEST					
N/RESOLUTION: 0					
Apply a 0-5 V, 100 Hz square wave to the rear panel GATE CONTROL connector.					
Set GATE DELAY Switch to  (right).		U46-5	C	Figures 2.19 & 2.20	Waveform 5
N/RESOLUTION: 4		U46-5	C	Figures 2.19 & 2.20	Waveform 6
Connect oscilloscope channel A to TP6. Connect the B+ GATE of oscilloscope to GATE CONTROL. Set oscilloscope to A. INTENSIFIED DURING B and B STARTS AFTER DELAY TIME. Set oscilloscope vertical input to CHOPPED MODE.					

Table 2.9 - Measurement Gate and Gate Control Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
		U22-5	D	Figures 2.19 & 2.20	Waveform 7
		U61-10	E	Figures 2.19 & 2.20	Waveform 8
Set GATE DELAY		U24-11	F	Figures 2.19 & 2.20	Waveform 9
switch to center position.		U61-10	E	Figures 2.19 & 2.20	Waveform 10
TEST/COM/SEP: TEST		U61-15	F	Figures 2.19 & 2.20	Waveform 10
N/RESOLUTION: 3		TP16	G	Figures 2.19 & 2.20	Waveform 11
		U10-3	H	Figures 2.19 & 2.20	Waveform 12
		TP10	I	Figures 2.19 & 2.20	Waveform 13
		U30-8	J	Figures 2.19 & 2.20	Waveform 14
		TP2	K	Figures 2.19 & 2.20	Waveform 15
		U24-13	L	Figures 2.19 & 2.20	Waveform 15

1 (NO.)

U62-3, 14



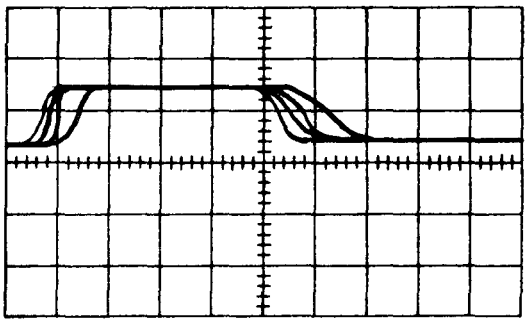
1 (V/DIV)

0.05 µS (S/DIV)

2 (NO.)

U62-3, 14

WIDTH 0.8 mS



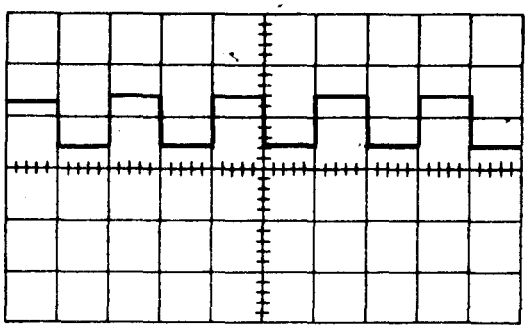
1 (V/DIV)

0.2 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

3 (NO.)

U62-3, 14



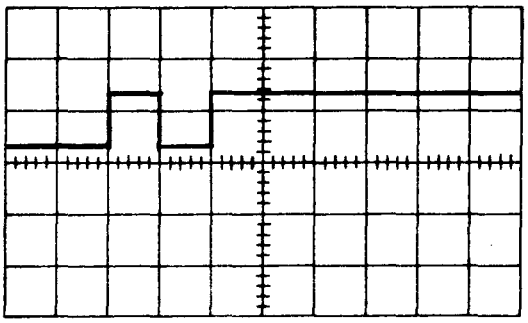
1 (V/DIV)

50 (S/DIV)

4 (NO.)

U62-3, 14

GATE TIME



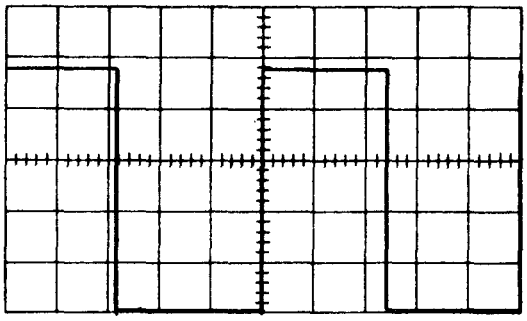
1 (V/DIV)

0.5 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

5 (NO.)

U46-5

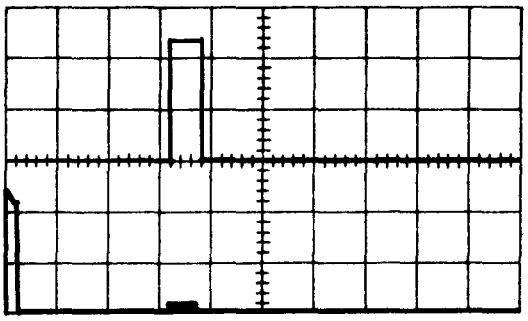


1 (V/DIV)

2 mS (S/DIV)

6 (NO.)

U46-5



CH 2 -0V

2 (V/DIV)

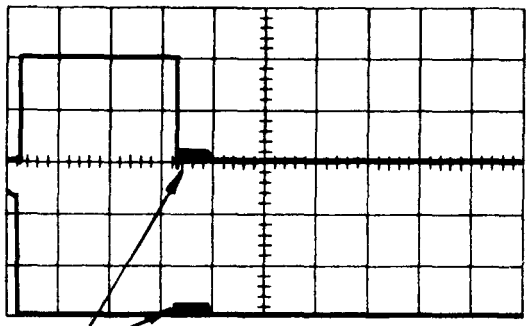
CH1 0V

0.5 mS (S/DIV)

B DELAYED SWEEP 20 µS/DIV

U22-5

7 (NO.)



2 (V/DIV)

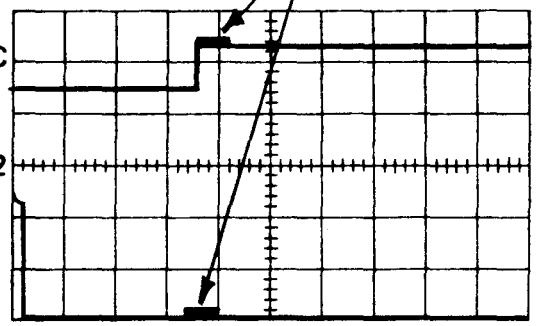
INTENSIFIED TRACE

0.5 mS (S/DIV)

U61-10

8 (NO.)

INTENSIFIED TRACE



ECL LOGIC LEVELS

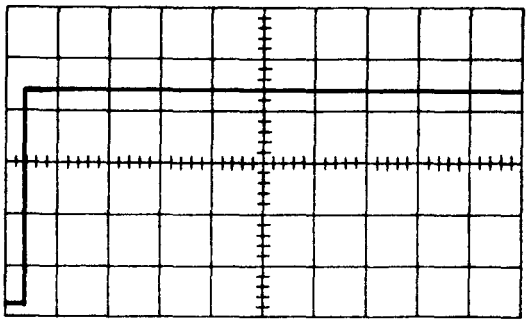
2 (V/DIV) CH 2

CH 1

0.5 mS (S/DIV)

U24-11

9 (NO.)



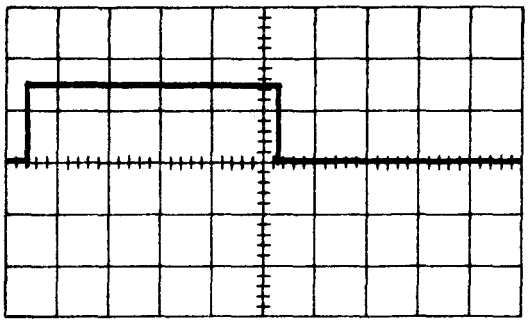
1 (V/DIV)

0.2 mS (S/DIV)

EST SYNC TO 6 + SLOPE

U61-10, 15

10 (NO.)



1 (V/DIV)

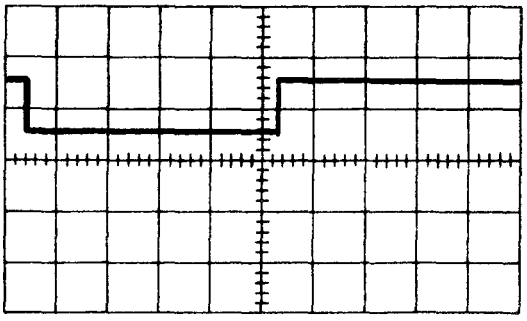
0.2 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

TP16

11 (NO.)

GATE TIME



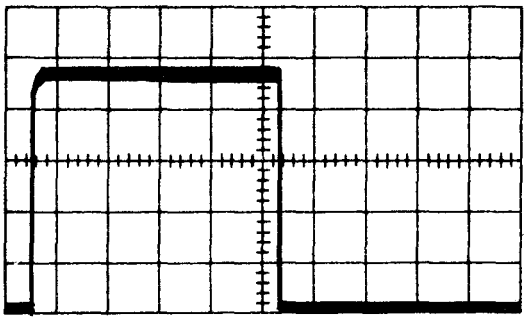
1 (V/DIV)

0.2 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

U10-3

12 (NO.)

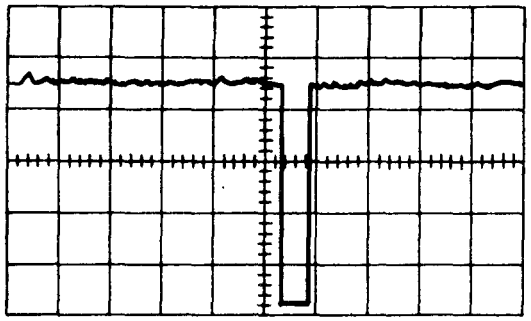


1 (V/DIV)

0.2 (S/DIV)

TP10

13 (NO.)



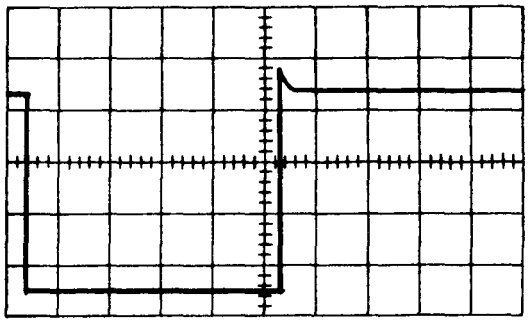
1 (V/DIV)

0.2 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

U30-8

14 (NO.)



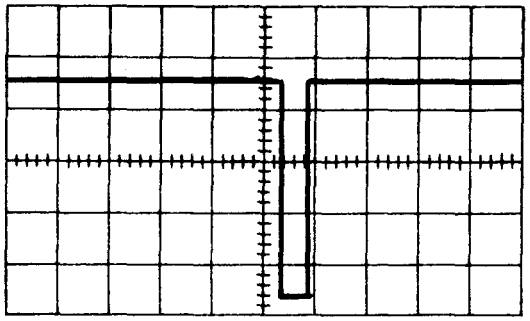
1 (V/DIV)

0.2 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

TP2, U24-13

15 (NO.)

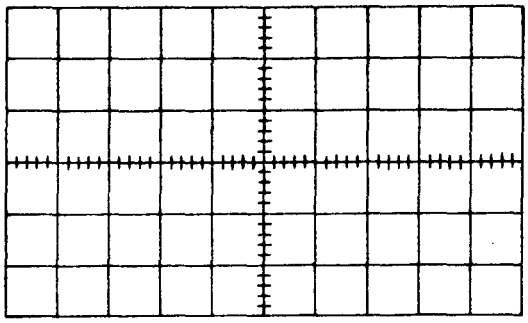


1 (V/DIV)

0.2 mS (S/DIV)

EXT SYNC TO TP6 + SLOPE

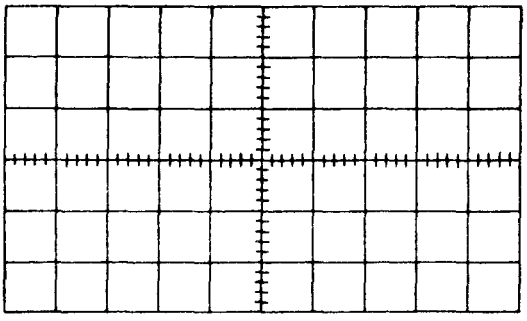
(NO.)



(V/DIV)

(S/DIV)

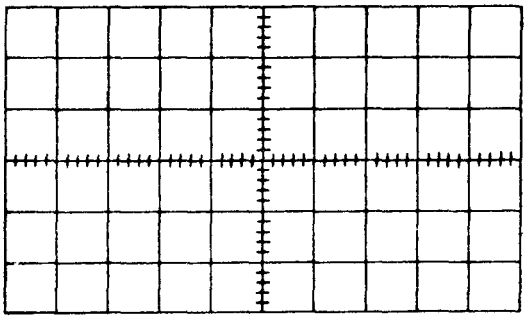
(NO.)



(V/DIV)

(S/DIV)

(NO.)



(V/DIV)

(S/DIV)

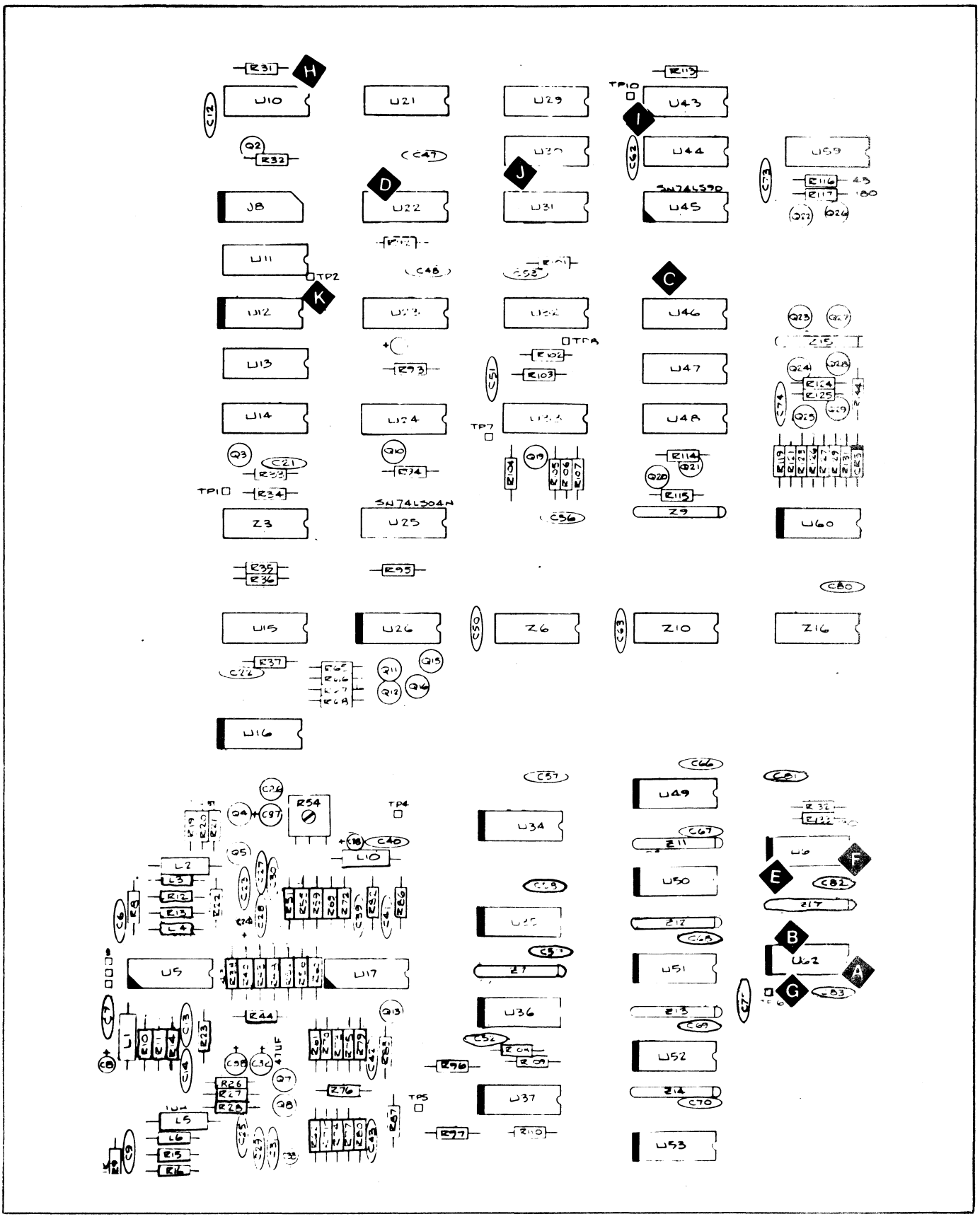


Figure 2.19 - Measurement Gate and Gate Control Test Point Locations

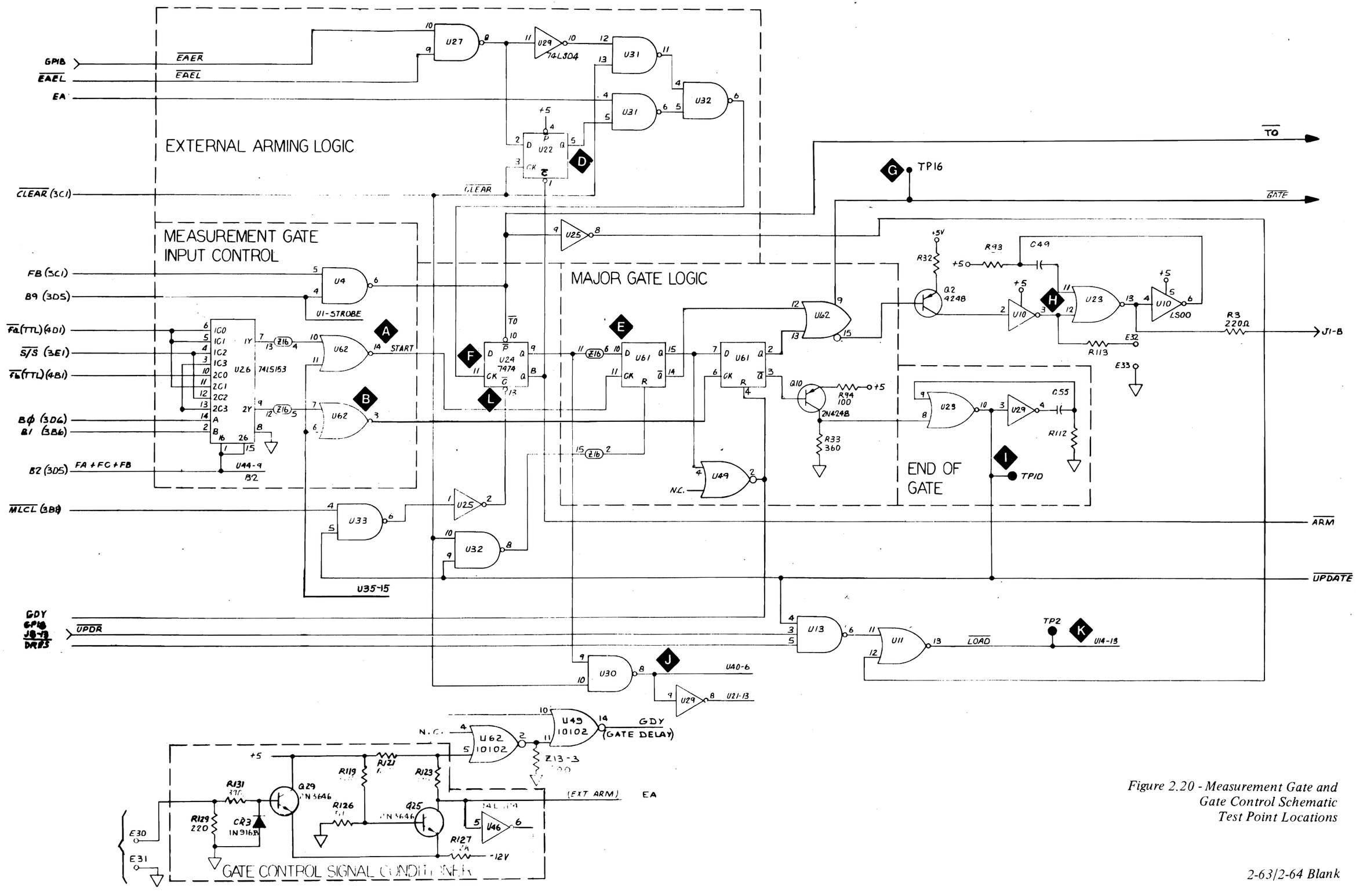


Figure 2.20 - Measurement Gate and Gate Control Schematic Test Point Locations

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Artek Media

Table 2.10 - Accumulator Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA N/RESOLUTION: 0 TEST/COM/SEP: COM RANGE: 1 INPUT CONTROLS: A B AC/DC: AC AC TRIGGER LEVEL PRESET PRESET Apply a 1 V RMS, 100 KHz sinewave to INPUT A.		TP13	A	Figures 2.21 & 2.22	Waveform 1
FUNCTION: P		TP13	A	Figures 2.21 & 2.22	Waveform 2
FUNCTION: F_B		TP13	A	Figures 2.21 & 2.22	Waveform 1
FUNCTION: TIA N/RESOLUTION: 7 INPUT CONTROLS: A B SLOPE: + – AC/DC AC AC TRIGGER LEVEL: PRESET PRESET		TP13	A	Figures 2.21 & 2.22	Waveform 3
FUNCTION: FA TEST/COM/SEP: TEST N/RESOLUTION: 7 SAMPLE RATE: Maximum		U52-2	B	Figures 2.21 & 2.22	Waveform 4
		U19-8	C	Figures 2.21 & 2.22	Waveform 5
		U9-28	D	Figures 2.21 & 2.22	Waveform 6

Table 2.10 - Accumulator Performance Test continued

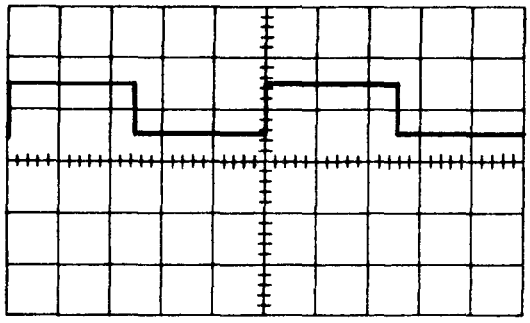
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
		U8-14	E	Figures 2.21 & 2.22	Waveform with a period of 1 second 80% duty cycle.
FUNCTION: FA		U9-22	F	Figures 2.21 & 2.22	Waveform 7
N/RESOLUTION: 2		U9-2	G	Figures 2.21 & 2.22	Waveform 8
TEST/COM/SEP: TEST		U9-3	H	Figures 2.21 & 2.22	Waveform 8
		U9-4	I	Figures 2.21 & 2.22	Waveform 8
		U9-5	J	Figures 2.21 & 2.22	Waveform 8
		U9-6	K	Figures 2.21 & 2.22	Waveform 8
		U9-7	L	Figures 2.21 & 2.22	Waveform 8
		U9-8	M	Figures 2.21 & 2.22	Waveform 8
		U9-9	N	Figures 2.21 & 2.22	Waveform 8
		U9-10	O	Figures 2.21 & 2.22	Waveform 9
		U2-6	P	Figures 5.21 & 2.22	Waveform 10
		U2-4	Q	Figures 2.21 & 2.22	Waveform 11
		U23-3	R	Figures 2.21 & 2.22	Waveform 11

TP-13

1 (NO.)

ECL LOGIC LEVELS

1 (V/DIV)

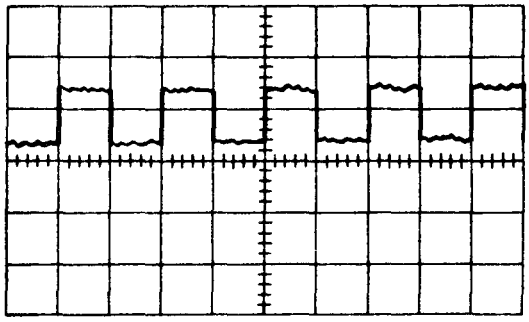


2 μS (S/DIV)

TP-13

2 (NO.)

1 (V/DIV)



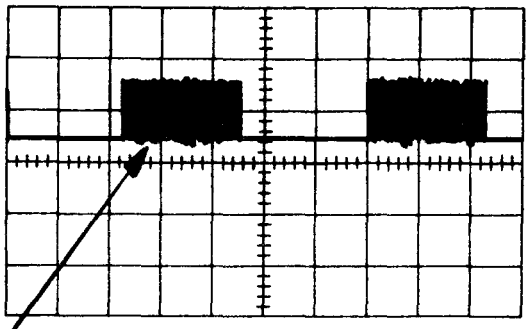
0.05 μS (S/DIV)

TP13

3 (NO.)

TIME INTERVAL UNDER MEASUREMENT

1 (V/DIV)



10 MHz REFERENCE CLOCK

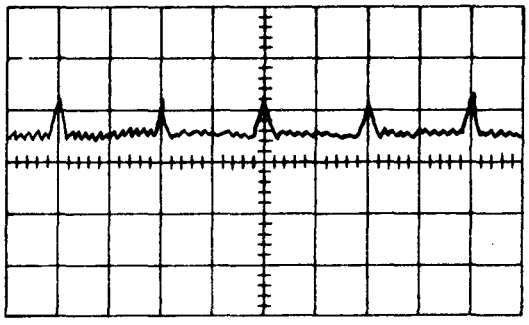
2 μS (S/DIV)

EXT SYNC TO U26-6

U52-2

4 (NO.)

1 (V/DIV)

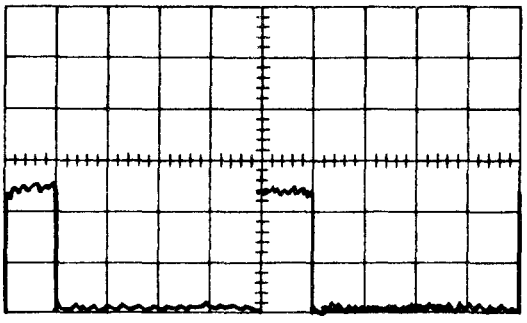


0.05 μS (S/DIV)

U19-8

5 (NO.)

1 (V/DIV)

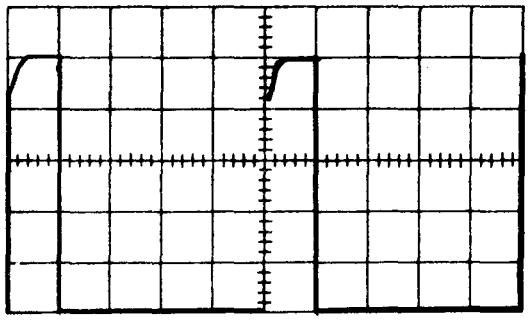


0.2 μS (S/DIV)

U9-28

6 (NO.)

1 (V/DIV)

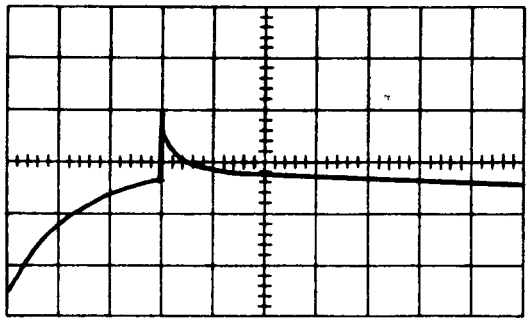


2 μS (S/DIV)

Waveforms for Table 2.10 continued

U9-22

7 (NO.)

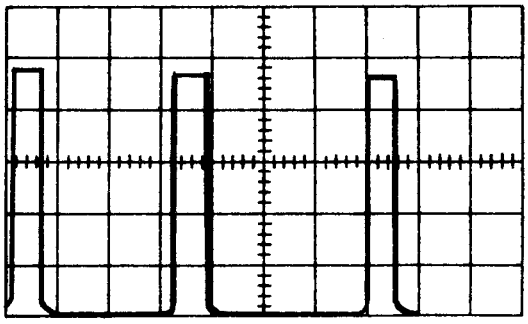


2 (V/DIV)

20 μS (S/DIV)

U9-2

8 (NO.)



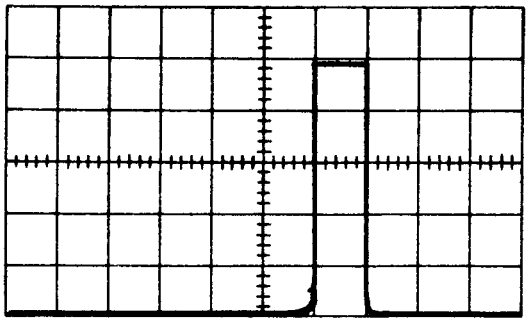
1 (V/DIV)

+SLOPE
EXT SYNC TO U1-3
WITH X10 PROBE

20 μS (S/DIV)

U9-10

9 (NO.)



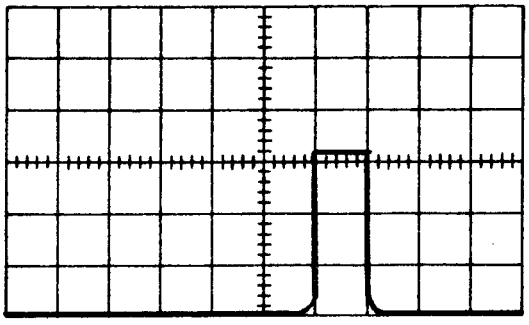
1 (V/DIV)

+ SLOPE
EXT SYNC TO U1-3
WITH X10 PROBE

10 μS (S/DIV)

U2-6

10 (NO.)

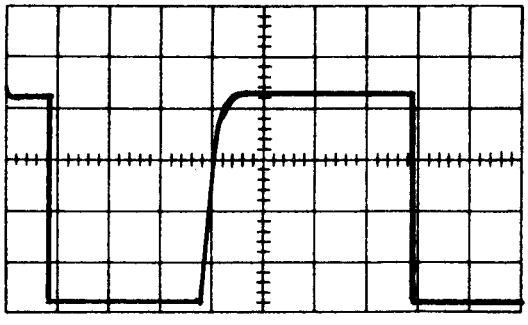


1 (V/DIV)

10 μS (S/DIV)

U2-4, U23-3

11 (NO.)

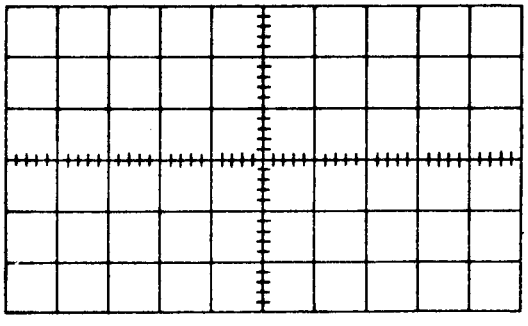


1 (V/DIV)

10 μS (S/DIV)

EXT SYNC TO U1-3
WITH X10 PROBE

(NO.)



(V/DIV)

(S/DIV)

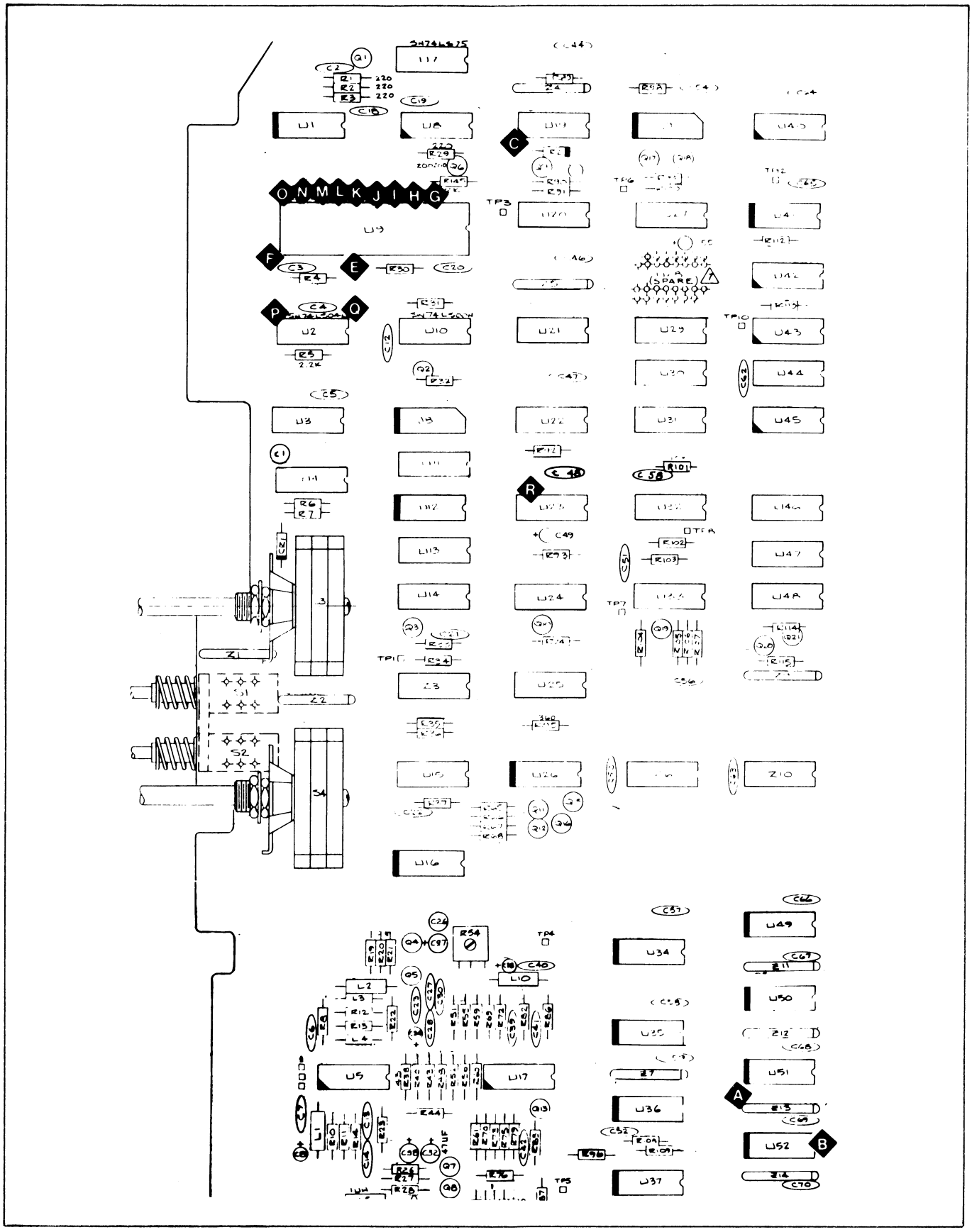


Figure 2.21 - Accumulator Test Point Locations

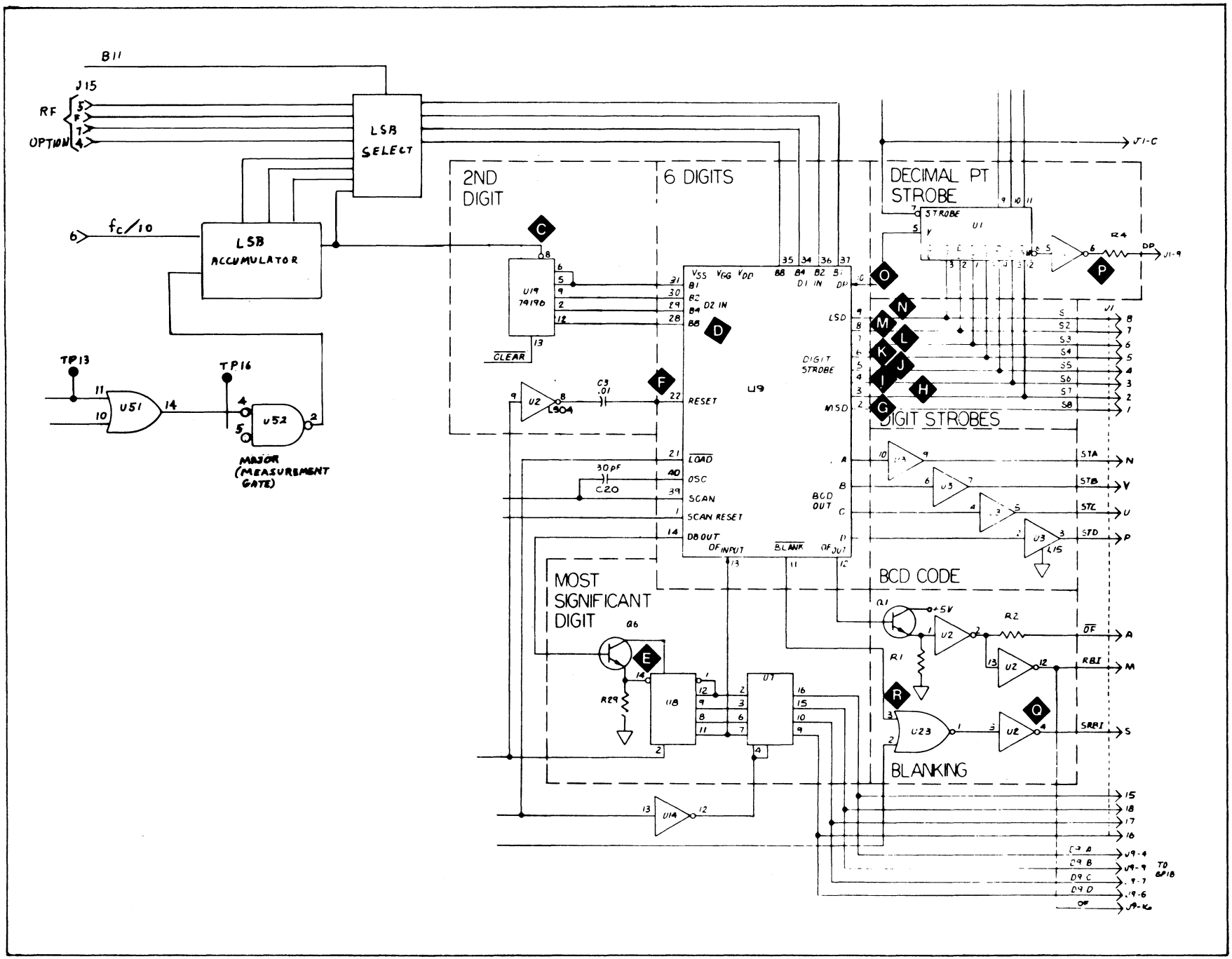


Figure 2.22 - Accumulator Schematic Test Point Locations

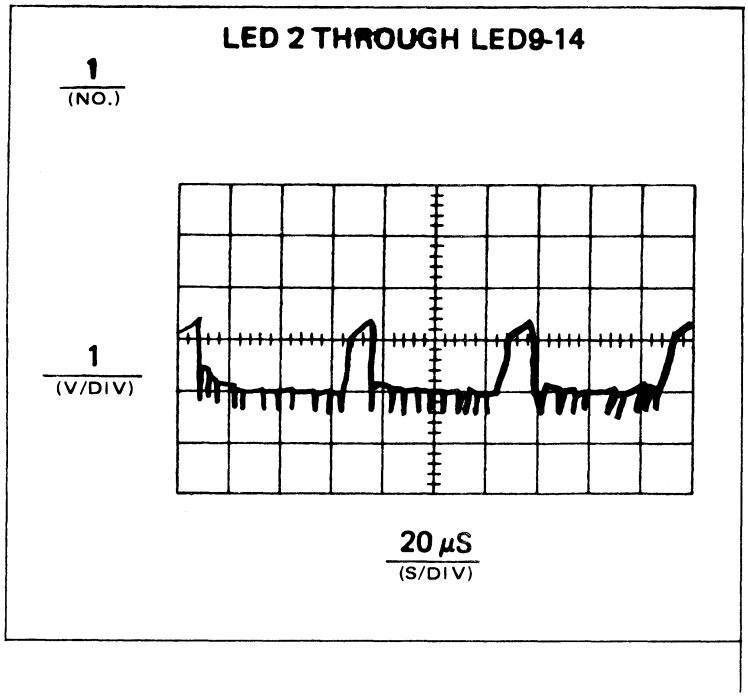
Table 2.11 - Display Logic Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA N/RESOLUTION: 7 TEST/COM/SEP: TEST INPUT CONTROLS: A B SLOPE: + – AC/DC: DC DC TRIGGER LEVEL: PRESET PRESET RANGE: 1 1		LED2-14	A	Figures 2.23 & 2.24	Waveform 1
		LED2-14		Figures 2.23 & 2.24	Waveform 1
		LED9-14		Figures 2.23 & 2.24	Waveform 1
N/RESOLUTION: 0		U4-9	B	Figures 2.23 & 2.24	∿0.4 Vdc
N/RESOLUTION: 4		U4-7	C	Figures 2.23 & 2.24	∿0.4 Vdc
N/RESOLUTION: 6		U4-6	D	Figures 2.23 & 2.24	∿0.4 Vdc
FUNCTION: P N/RESOLUTION: 0		U4-2	E	Figures 2.23 & 2.24	∿0.4 Vdc
N/RESOLUTION: 3		U4-4	F	Figures 2.23 & 2.24	∿0.4 Vdc
N/RESOLUTION: 5		U4-5	G	Figures 2.23 & 2.24	∿0.4 Vdc
FUNCTION: PA N/RESOLUTION: 5		U4-3	H	Figures 2.23 & 2.24	∿0.4 Vdc
FUNCTION: FA N/RESOLUTION: 6 TEST/COM/SEP: TEST SAMPLE RATE: HOLD PRESS RESET and RELEASE		CRI Cathode	I	Figures 2.23 & 2.24	4 Vdc Drop to 2.8 Vdc for 1 second and returns to 4 Vdc

Table 2.11 - Display Logic Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: TOT TEST/COM/SEP: TEST Press START Switch.		Cathode CR9	J	Figures 2.23 & 2.24	4 Vdc after 100 second, drops to 3 Vdc.

Waveform for Table 2.11



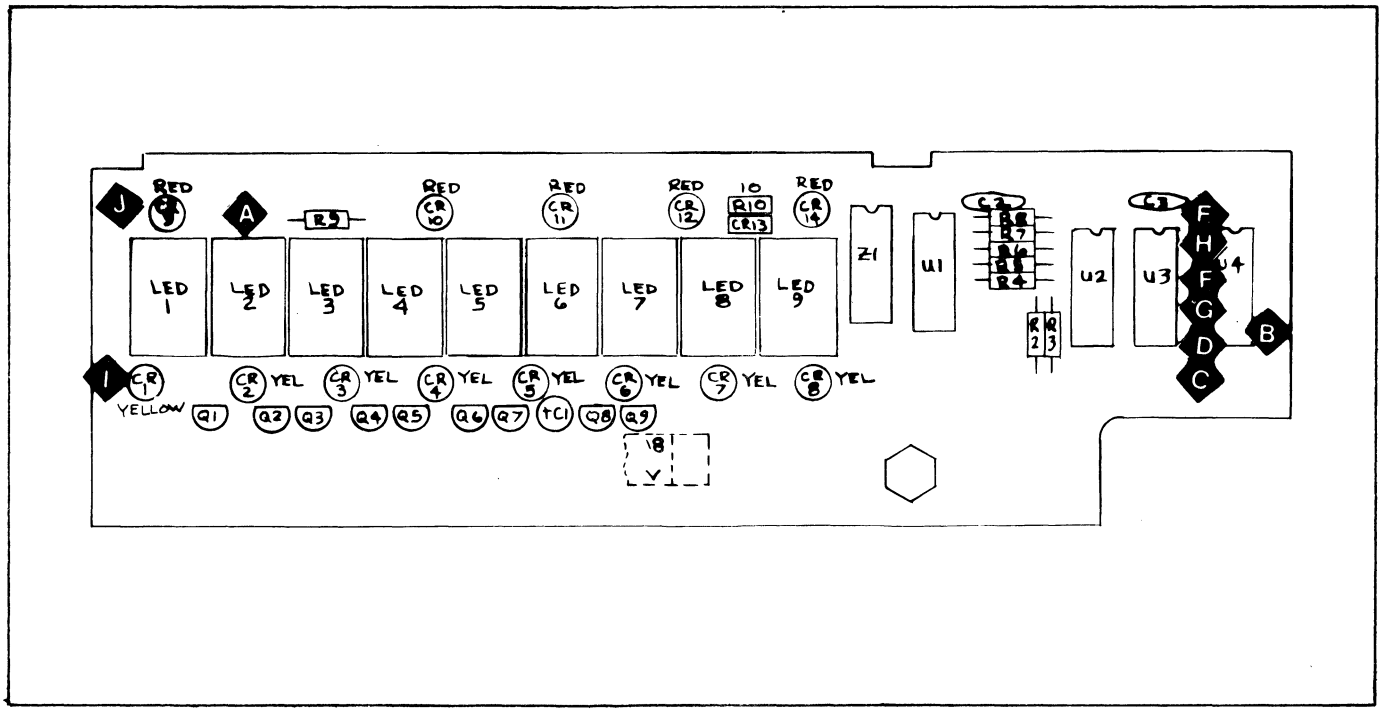


Figure 2.23 - Display Logic Board Test Point Locations

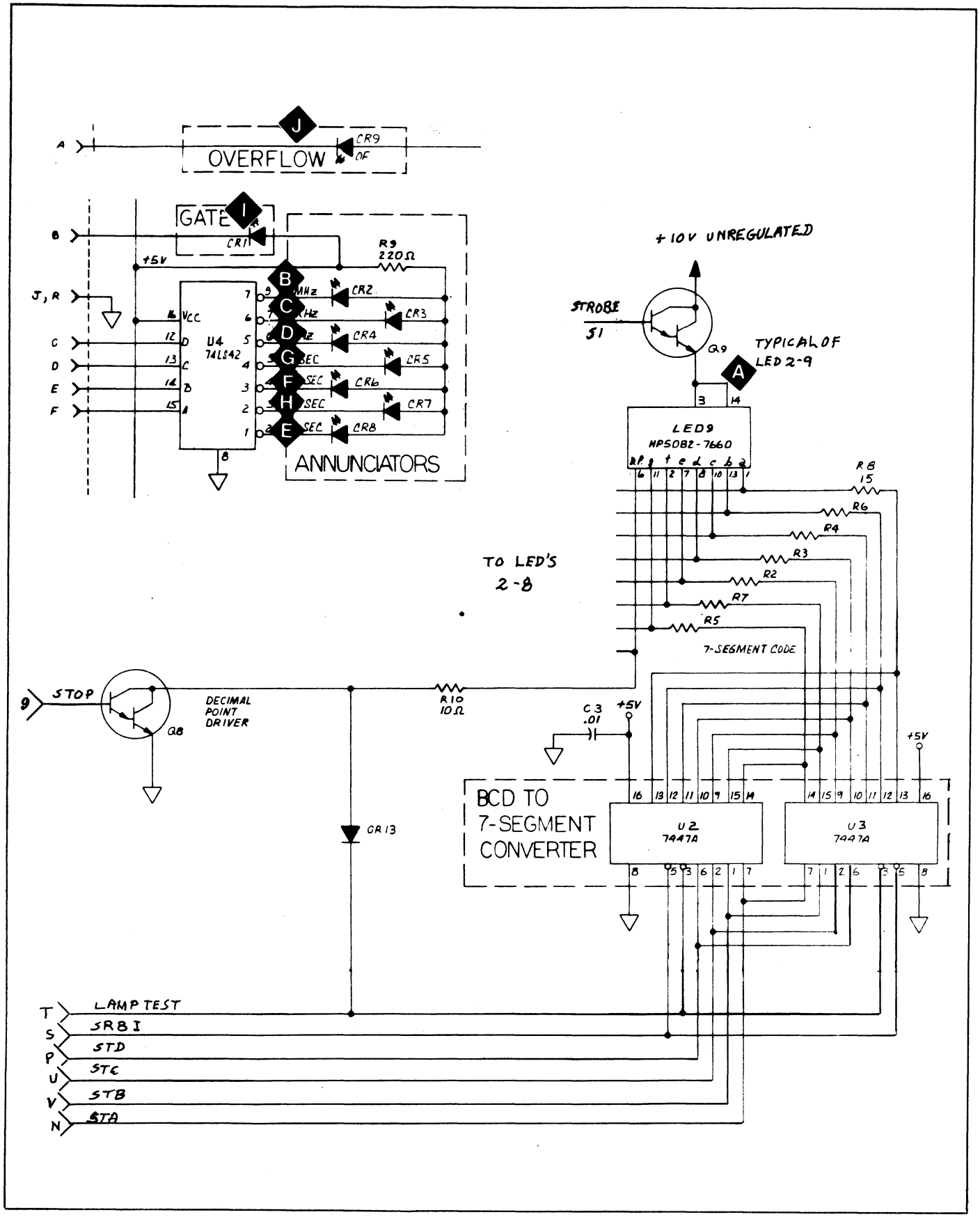


Figure 2.24 - Display Logic Schematic Test Point Locations

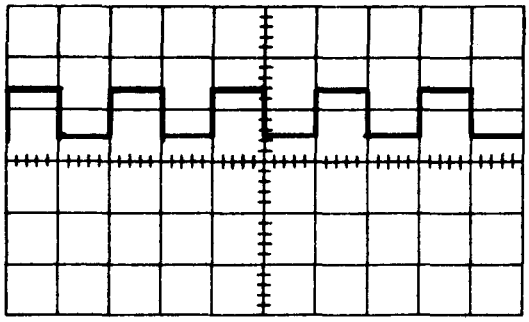
Table 2.12 - TIA Synchronizer and Marker Generator Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
F UNCTION: TIA N/RESOLUTION: 7 TEST/COM/SEP: COM INPUT CONTROLS: A B SLOPE: + – AC/DC AC AC TRIGGER LEVEL: PRESET PRESET RANGE: 1 1 Apply a 1 VRMS, 100 KHz sinewave toINPUT INPUT A.		TP9	A	Figures 2.25 & 2.26	Waveform 1
		TP14	B	Figures 2.25 & 2.26	Waveform 1
		U59-3	C	Figures 2.25 & 2.26	Waveform 2
		U59-11	D	Figures 2.25 & 2.26	Waveform 2
		U26-6	E	Figures 2.25 & 2.26	Waveform 2
		U26-10	F	Figures 2.25 & 2.26	Waveform 2
		U59-6	G	Figures 2.25 & 2.26	Waveform 3
		U59-8	H	Figures 2.25 & 2.26	Waveform 4
		U52-14	I	Figures 2.25 & 2.27	Waveform 5
		U39-3	J	Figures 2.25 & 2.27	Waveform 6
N/RESOLUTION: 7		U54-14	K	Figures 2.25 & 2.27	Waveform 7
		U36-11	L	Figures 2.25 & 2.27	Waveform 8
		U38-11	M	Figures 2.25 & 2.27	Waveform 8
		U54-12	N	Figures 2.25 & 2.27	Waveform 8
		U48-5	O	Figures 2.25 & 2.27	Waveform 9
		U39-4	P	Figures 2.25 & 2.27	Waveform 8
		U39-2	Q	Figures 2.25 & 2.27	Waveform 10

Waveforms for Table 2.12

TP9, TP14

1 (NO.)

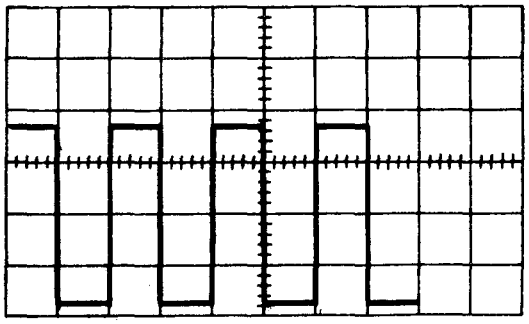


1 (V/DIV)

5 µS (S/DIV)

U26-6, 10

2 (NO.)

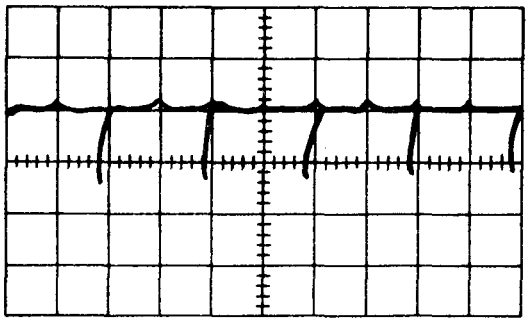


1 (V/DIV)

5 µS (S/DIV)

U59-6

3 (NO.)

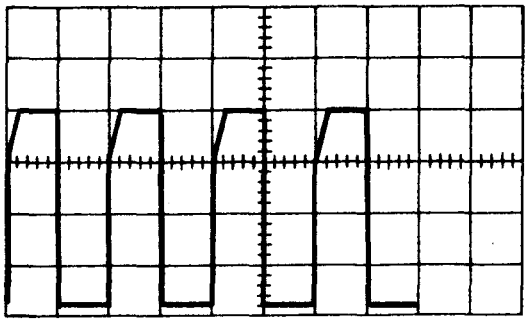


1 (V/DIV)

5 µS (S/DIV)

U59-8

4 (NO.)

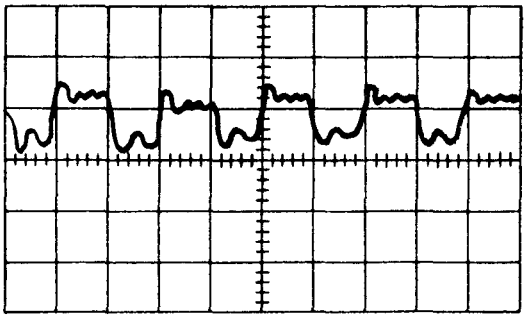


1 (V/DIV)

5 µS (S/DIV)

U52-14

5 (NO.)

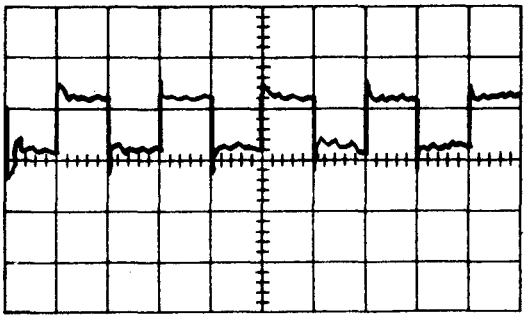


1 (V/DIV)

0.05 µS (S/DIV)

U39-3

6 (NO.)



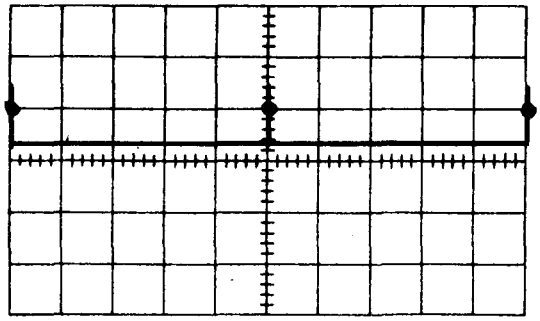
1 (V/DIV)

0.05 µS (S/DIV)

Waveforms for Table 2.12 continued

U54-14

7 (NO.)

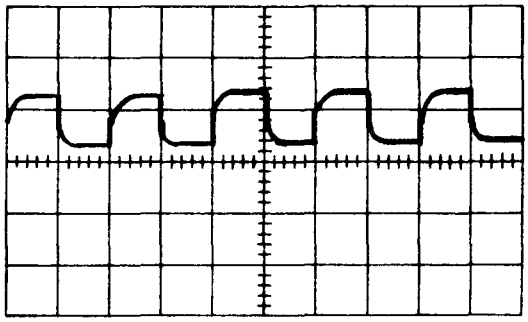


1 (V/DIV)

2 µS (S/DIV)

U36-11, U38-11, U54-12, U39-4

8 (NO.)

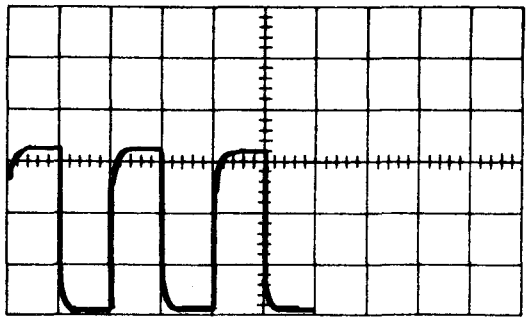


1 (V/DIV)

5 µS (S/DIV)

U48-5

9 (NO.)

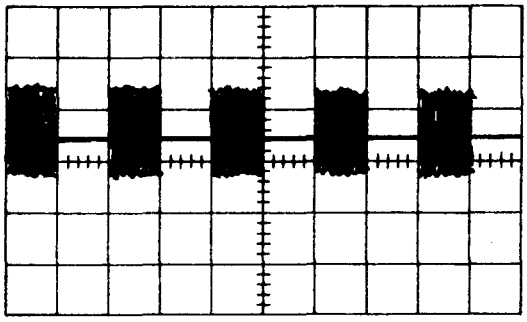


1 (V/DIV)

5 µS (S/DIV)

U39-2

10 (NO.)



1 (V/DIV)

5 µS (S/DIV)

EXT SYNC AT TP14 + SLOPE

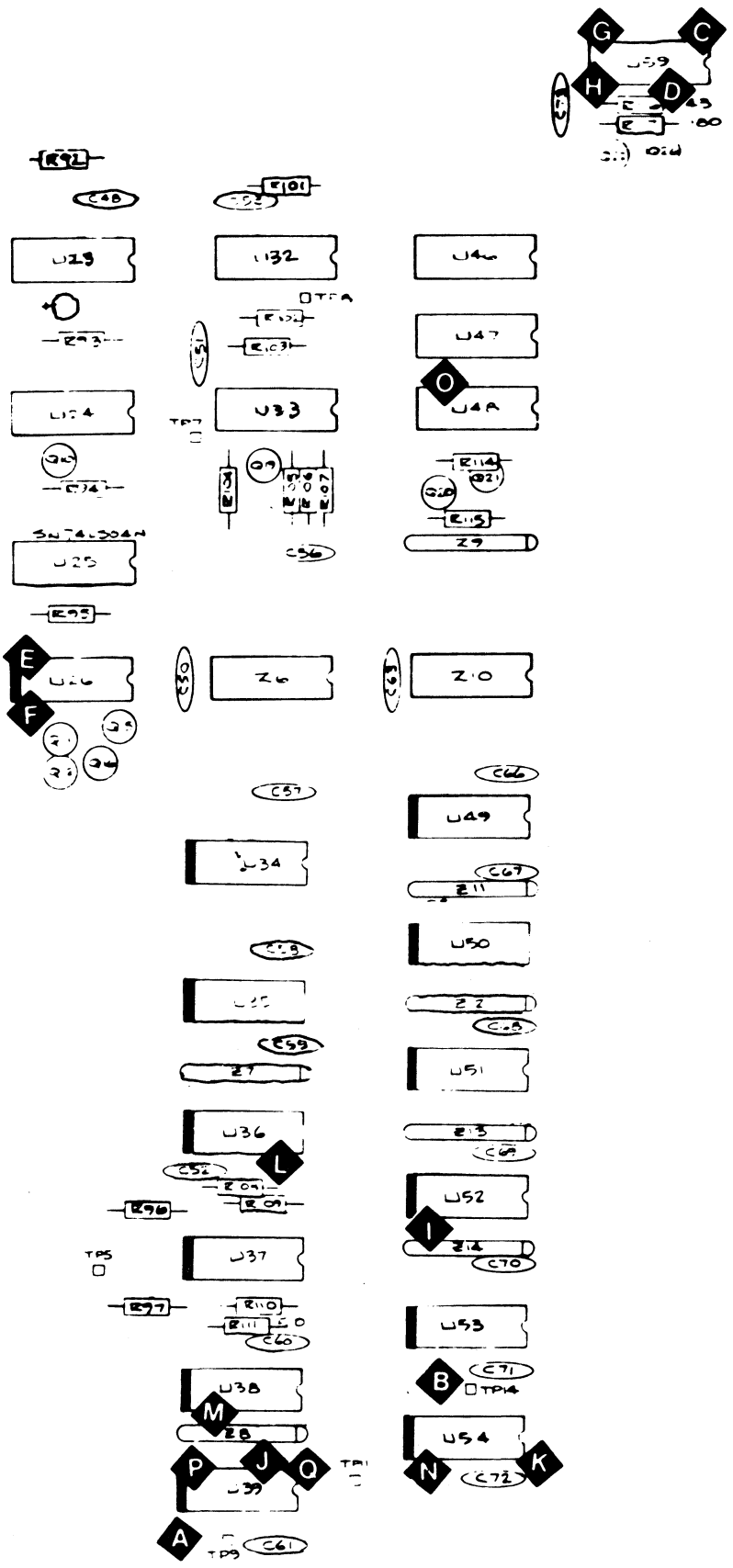


Figure 2.25 - TIA Synchronizer and Marker Generator Test Point Locations

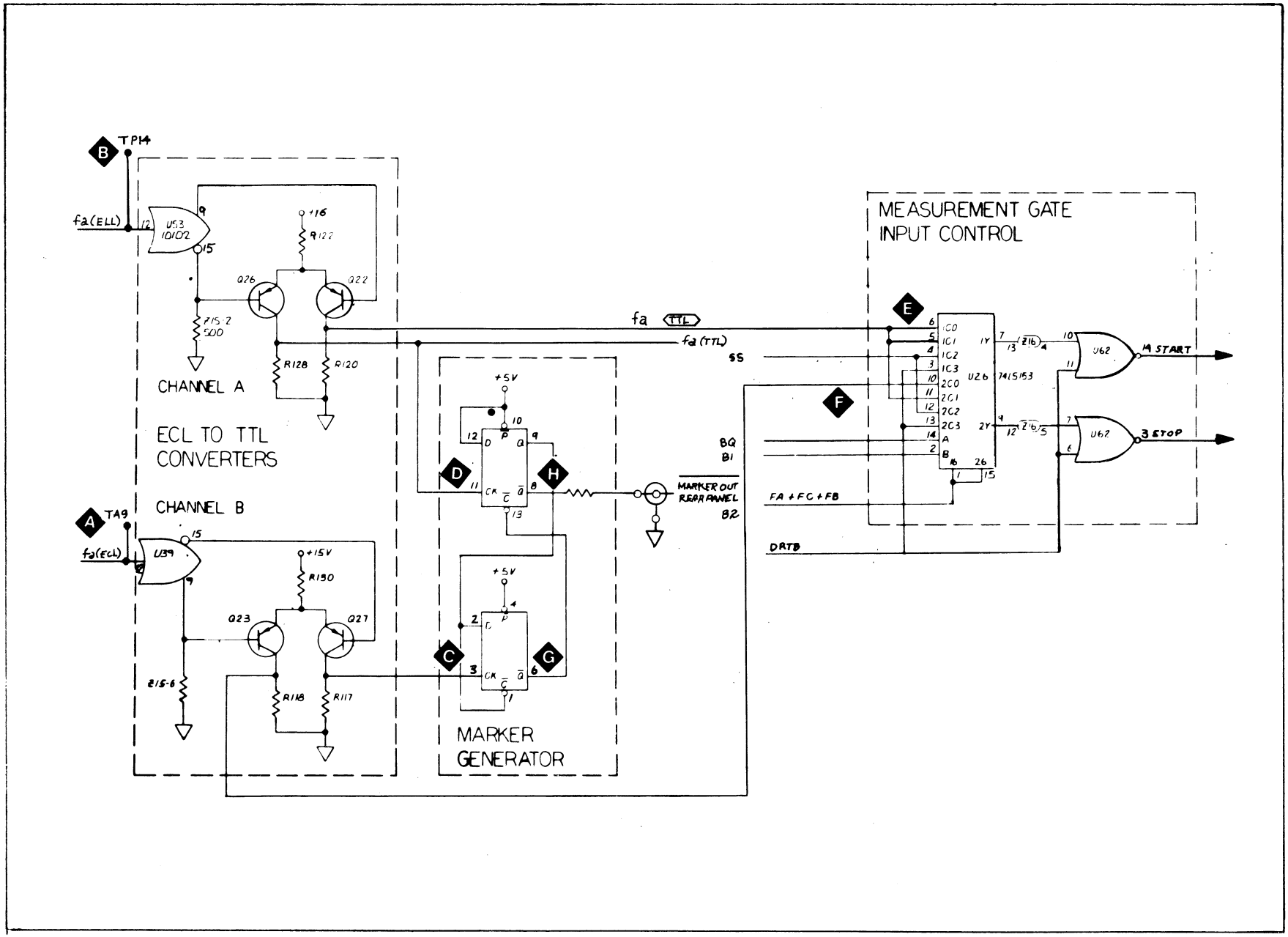


Figure 2.26 - Marker Generator Schematic Test Point Locations

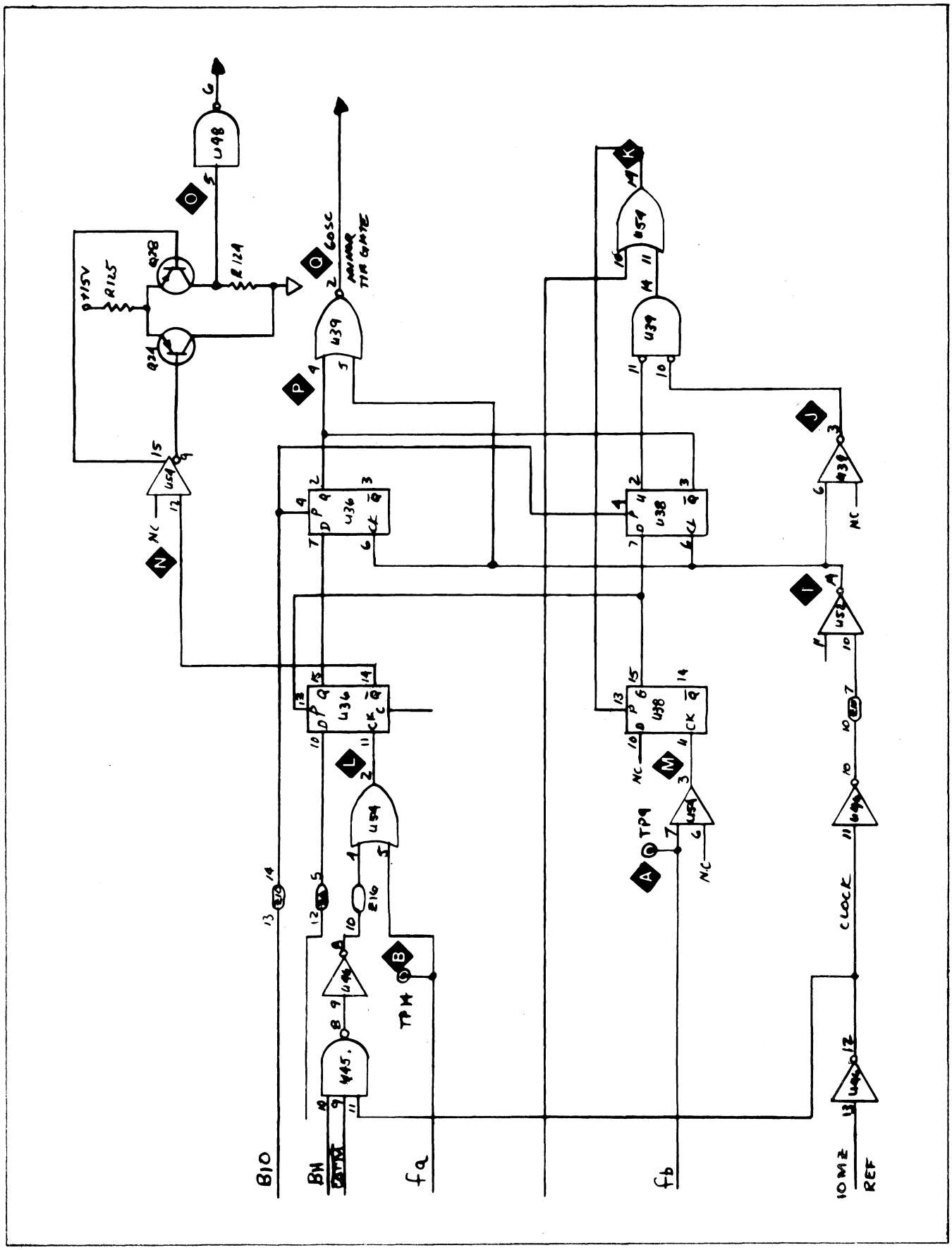


Figure 2.27 - TIA Synchronizer Schematic Test Point Locations

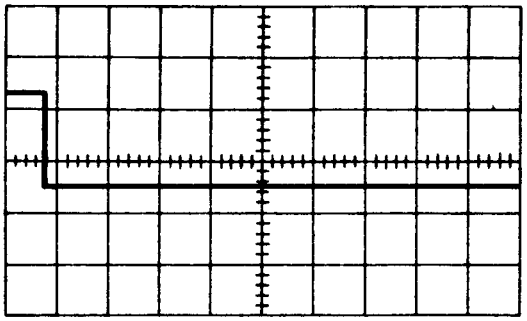
Table 2.13 - 50-512 MHz RF Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: F_C N/RESOLUTION: 3 TEST/COM/SEP: Apply a 2.5 V P-P 50 MHz sinewave to INPUT C. Remove the shield over the input components on the RF board.		U6-2	A	Figures 2.28 & 2.29	700 mV P-P sinewave
Reduce the input signal to 10 m V P-P		U4-4	B	Figures 2.28 & 2.29	1.8 V P-P sinewave
		U3-3	C	Figures 2.28 & 2.29	Waveform 1
		U3-16	D	Figures 2.28 & 2.29	Waveform 2
		U1-15	E	Figures 2.28 & 2.29	Waveform 2
		U1-12	F	Figures 2.28 & 2.29	Waveform 3
	Carry OUTPUT	U3-9	G	Figures 2.28 & 2.29	Waveform 3
		Q10 Collector	H	Figures 2.28 & 2.29	+5 Vdc
		U2-7	I	Figures 2.28 & 2.29	0 Vdc
Disconnect the input signal		Q10 Collector	J	Figures 2.28 & 2.29	0 Vdc
		U2-7	K	Figures 2.28 & 2.29	+5 Vdc

Waveforms for Table 2.13

U3-3

1 (NO.)



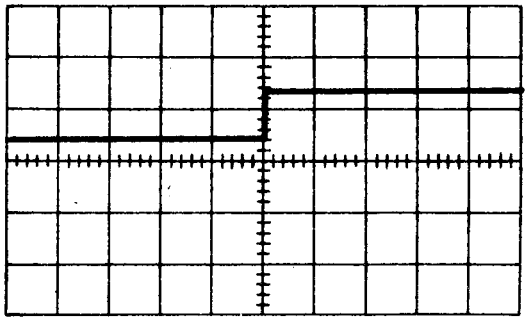
2 (V/DIV)

0.1 mS (S/DIV)

U3-16, U1-12, 15

2 (NO.)

GATE TIME



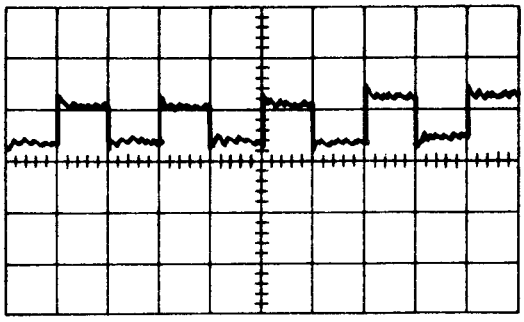
1 (V/DIV)

0.2 mS (S/DIV)

RISE TIME <2 nS AT U3-16

U3-9, U1-14

3 (NO.)



1 (V/DIV)

0.05 µS (S/DIV)

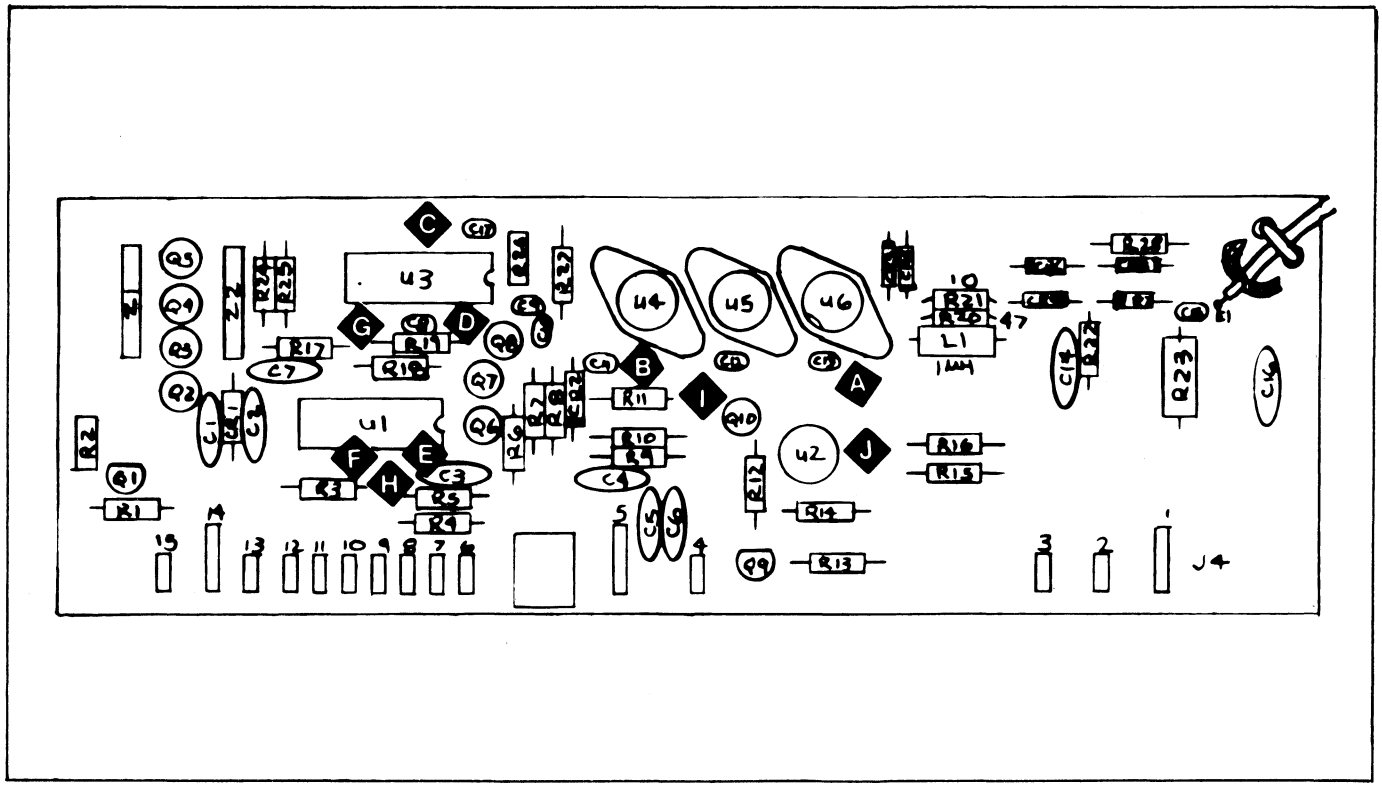


Figure 2.28 - 512 MHz Direct Count RF Board Test Point Locations

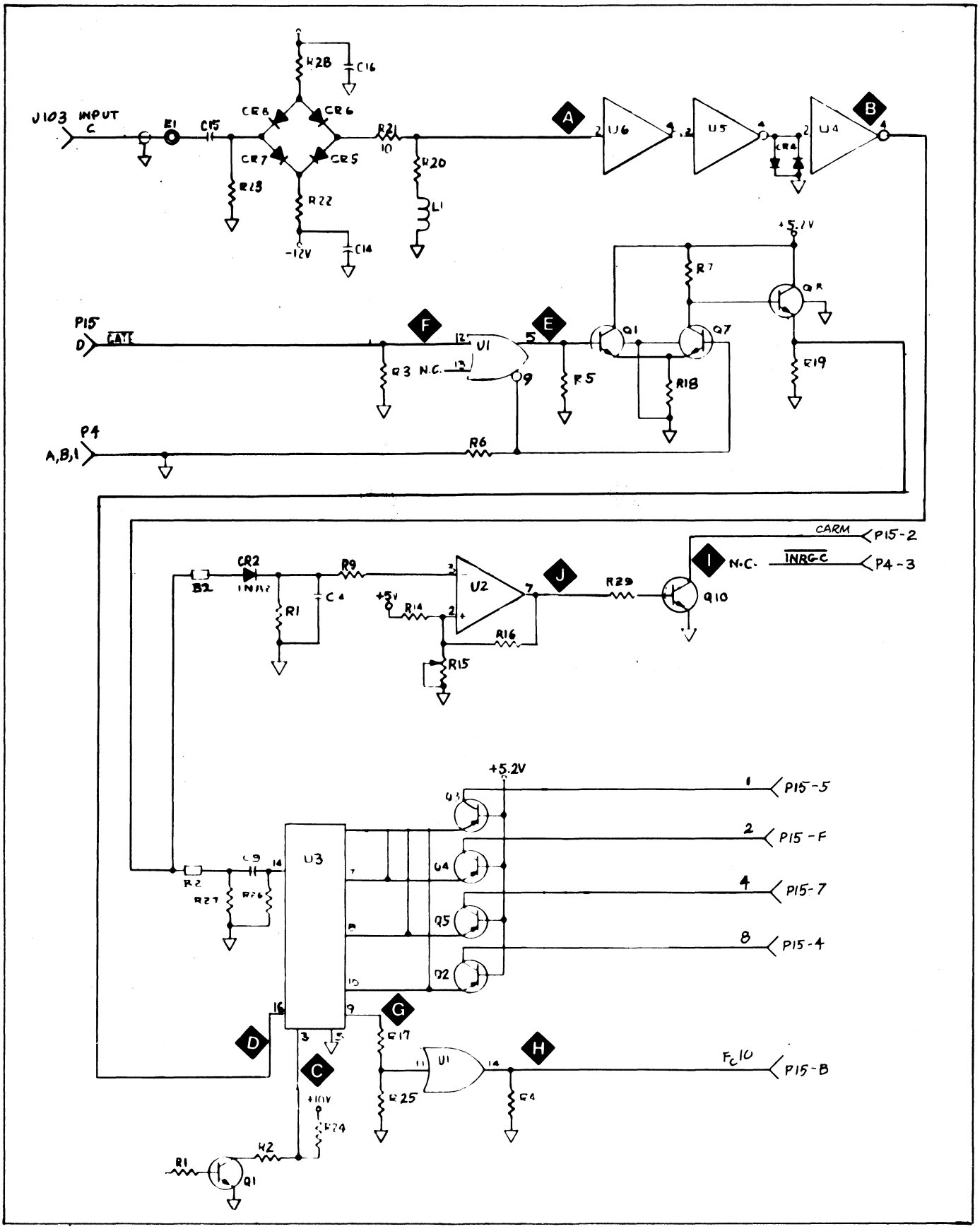


Figure 2.29 - 50-512 MHz RF Schematic Test Point Locations

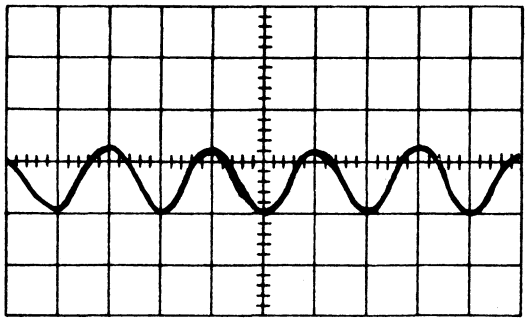
Table 2.14 - Reference Multiplier Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Apply a 1 VRMS 5 MHz ± 50 Hz sinewave to the REP rear panel connector.		Collector Q3	A	Figures 2.30 & 2.31	Waveform 1
		Collector Q4	B	Figures 2.30 & 2.31	Waveform 2
		Base Q2	C	Figures 2.30 & 2.31	Waveform 3
		Collector Q2	D	Figures 2.30 & 2.31	Waveform 4

Waveforms for Table 2.14

COLLECTOR Q3

1 (NO.)

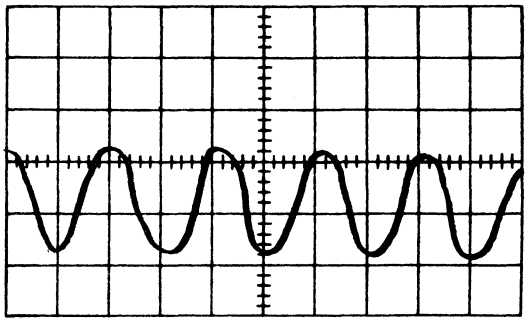


2 (V/DIV)

0.05 µS (S/DIV)

COLLECTOR Q4

2 (NO.)

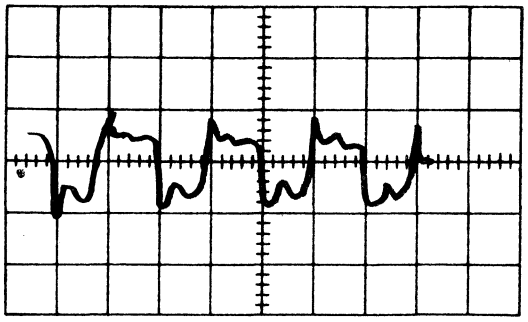


1 (V/DIV)

0.05 µS (S/DIV)

BASE Q2

3 (NO.)

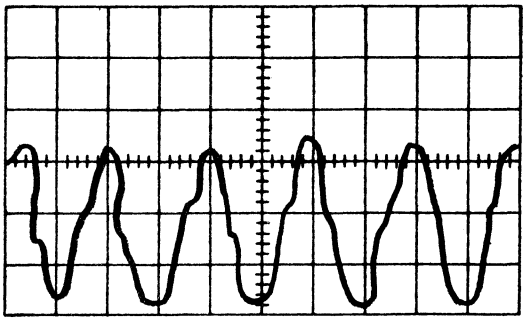


1 (V/DIV) OV

0.05 µS (S/DIV)

COLLECTOR Q2

4 (NO.)



1 (V/DIV)

0.05 µS (S/DIV)

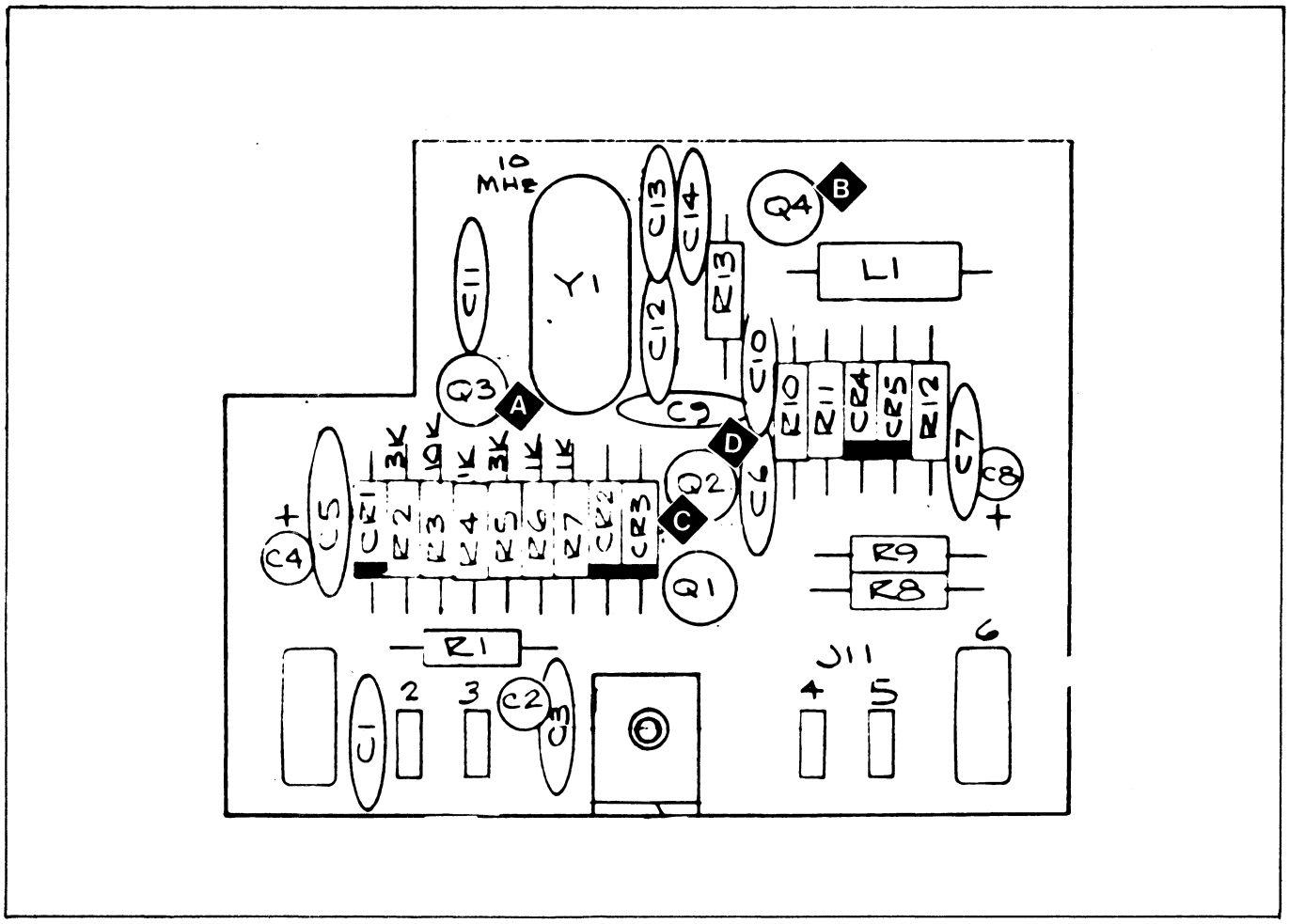


Figure 2.30 - Reference Multiplier Test Point Locations

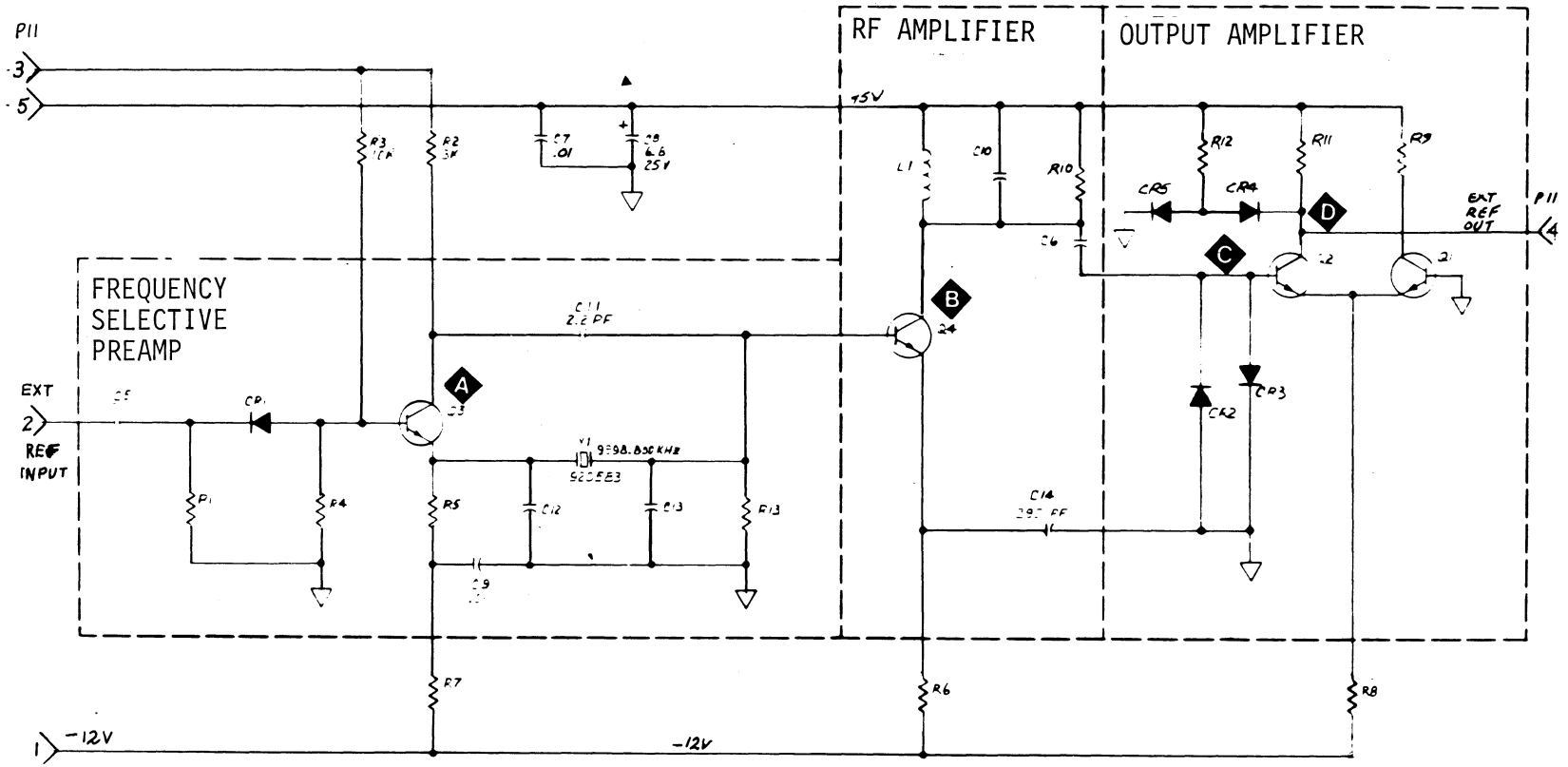
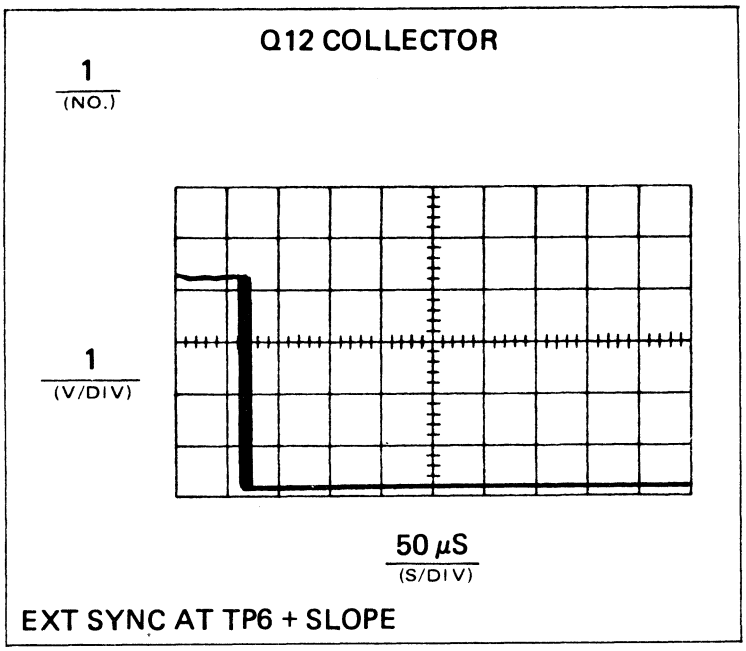


Figure 2.31 - Reference Multiplier Schematic Test Point Locations

Table 2.15 - Auto Trigger Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
FUNCTION: FA TEST/COM/SEP: SEP INPUT CONTROLS: A SLOPE: + No Input signal		U47-10	A	Figures 2.32 & 2.33	Low when the trigger level control is fully CCW and High when fully CW.
N/RESOLUTION: 3 INPUT CONTROLS: A SLOPE: + AC/DC: AC TRIGGER LEVEL: PRESET Apply a 1 VRMS, 100 KHz sinewave to INPUT A. SAMPLE RATE: Maximum		Q12 Collector	B	Figures 2.32 & 2.33	Waveform 1

Waveform for Table 2.15



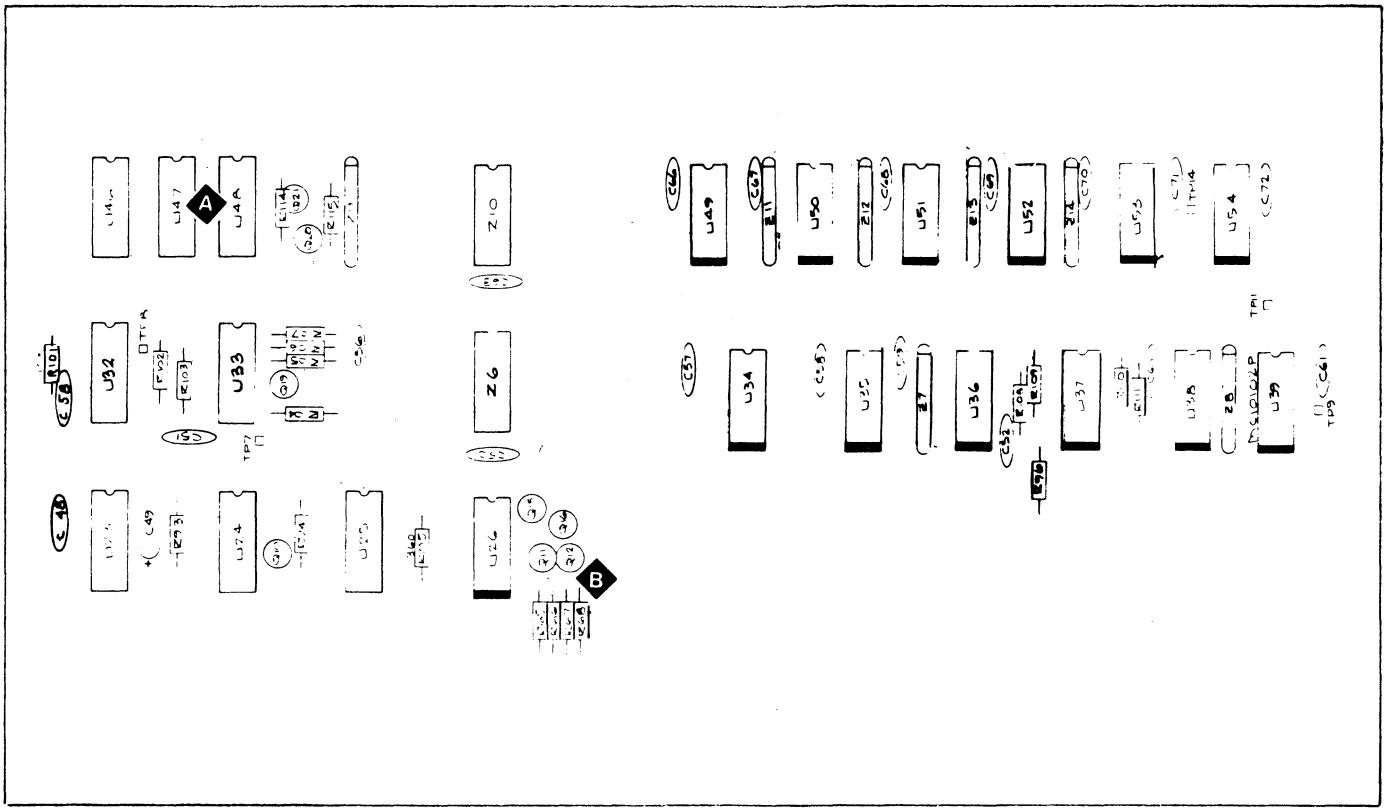


Figure 2.32 - Auto Trigger Test Point Locations

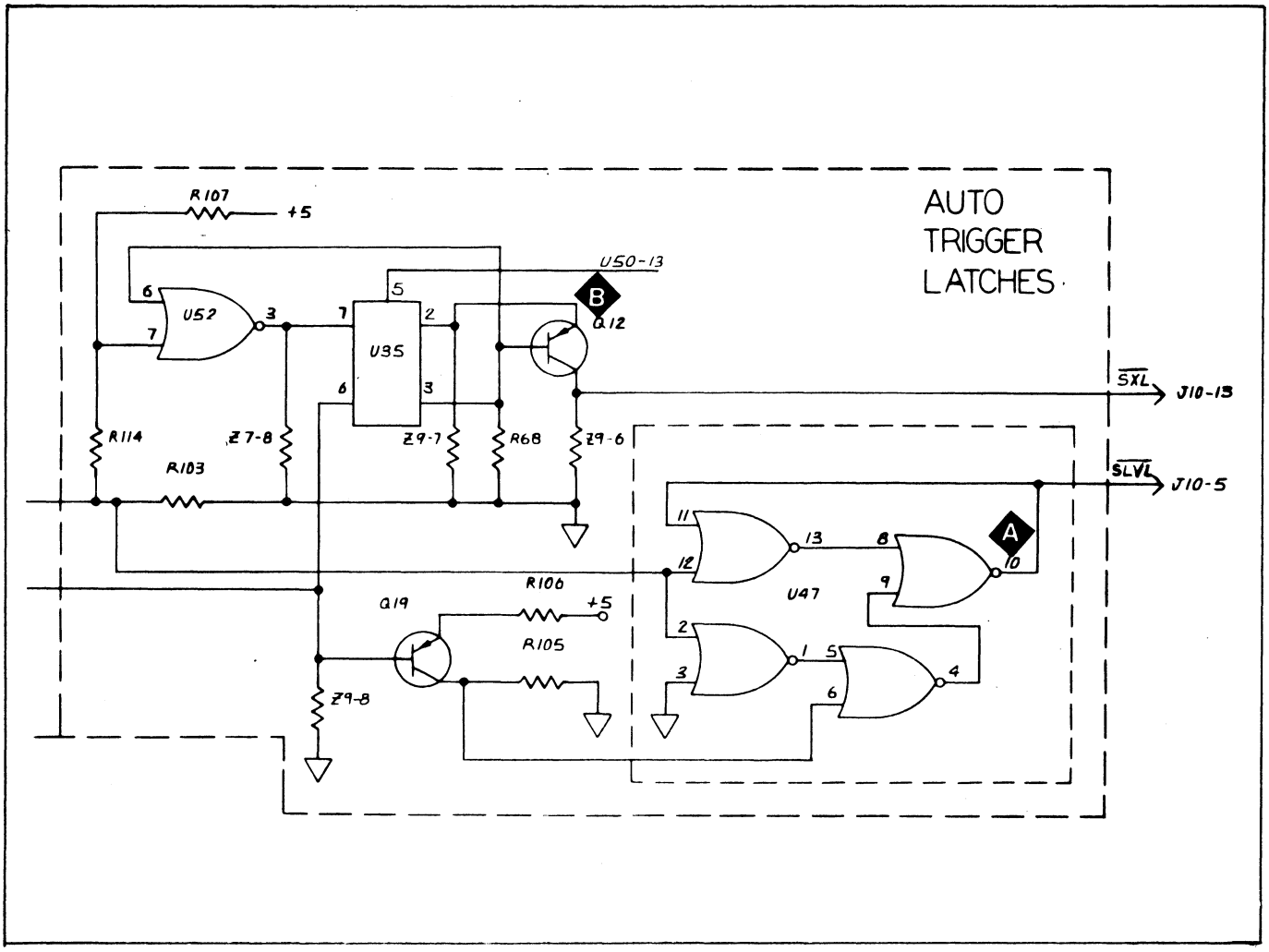


Figure 2.33 - Auto Trigger Schematic Test Point Locations

Table 2.16 - Power Supply Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
		Cathode CR8	1	Figures 2.34 & 2.35	Approximately +12 Vdc
		Cathode CR4	2	Figures 2.34 & 2.35	Approximately +23 Vdc
		Anode CR6	3	Figures 2.34 & 2.35	Approximately −24 Vdc
		TP18	4	Figures 2.34 & 2.35	+15.00 ± 0.25 Vdc
		TP19	5	Figures 2.34 & 2.35	−12.0 ± 0.6 Vdc
		TP21	6	Figures 2.34 & 2.35	+5.00 ± 0.25 Vdc
		TP22	7	Figures 2.34 & 2.35	+5.2 ± 0.3 Vdc
		GPIBTP11 (Ref TP10)	8		+5.00 ± 0.25 Vdc

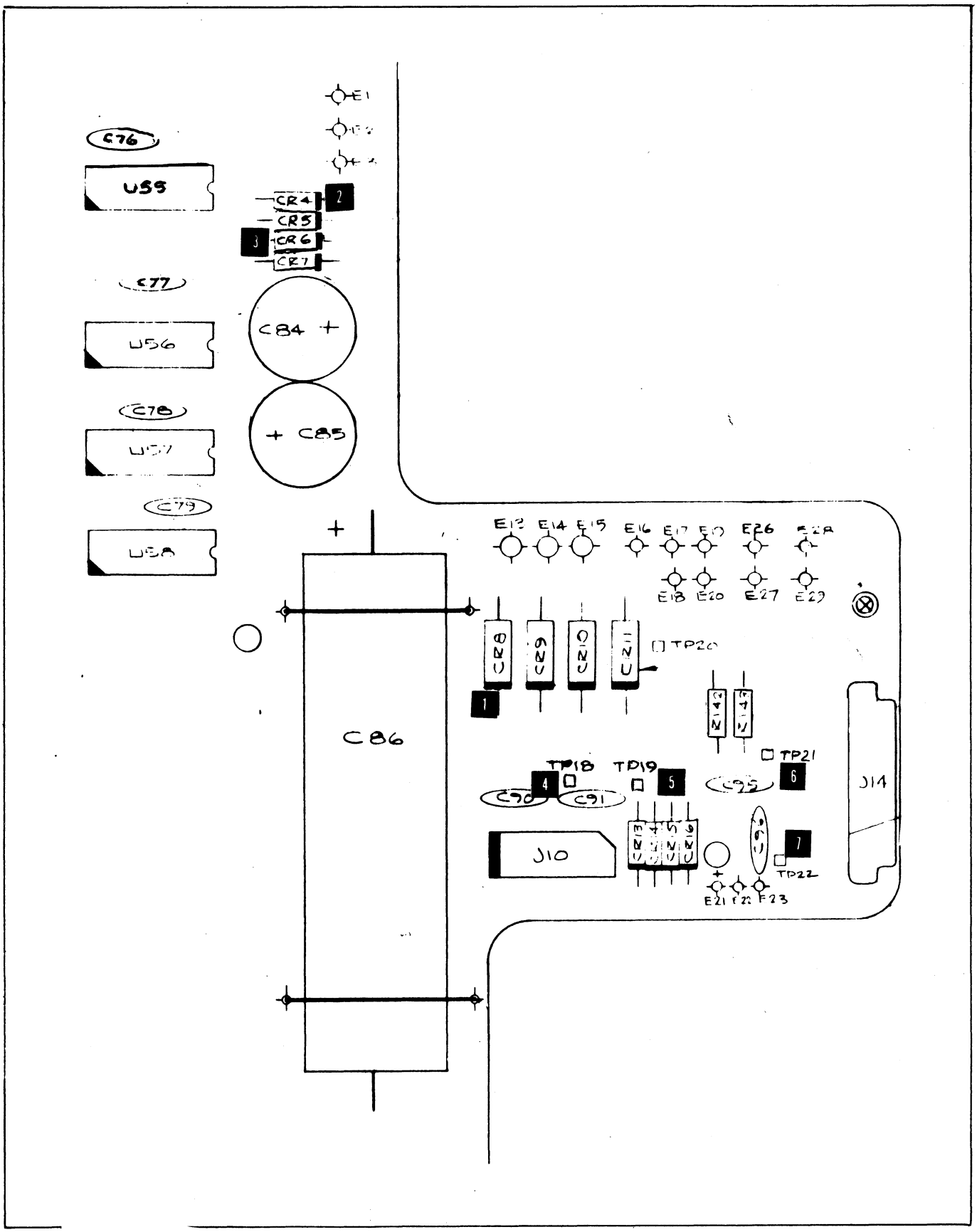


Figure 2.34 - Power Supply Test Point Locations

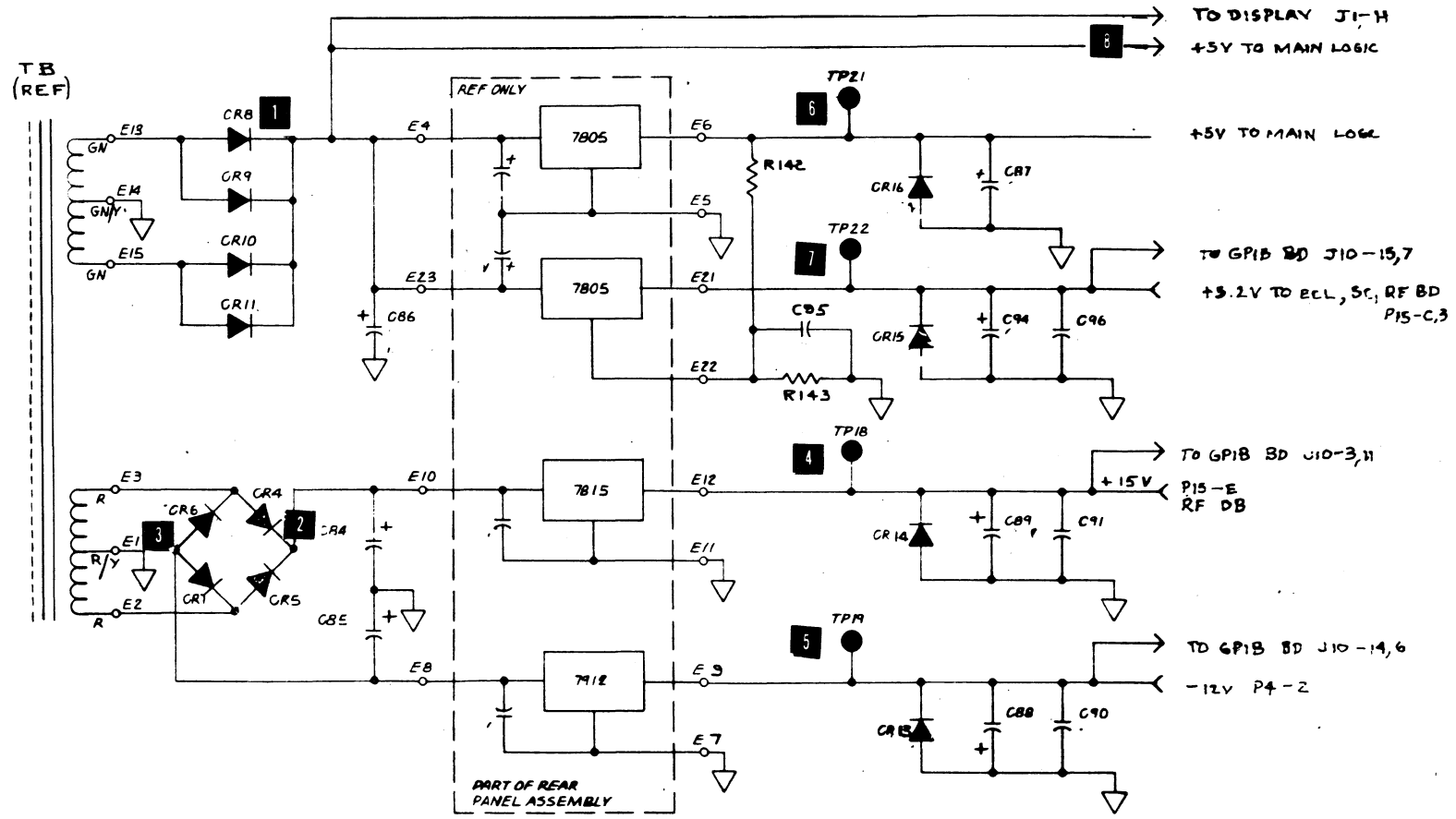


Figure 2.35 - Power Supply Schematic Test Point Locations

SECTION 3 DRAWINGS

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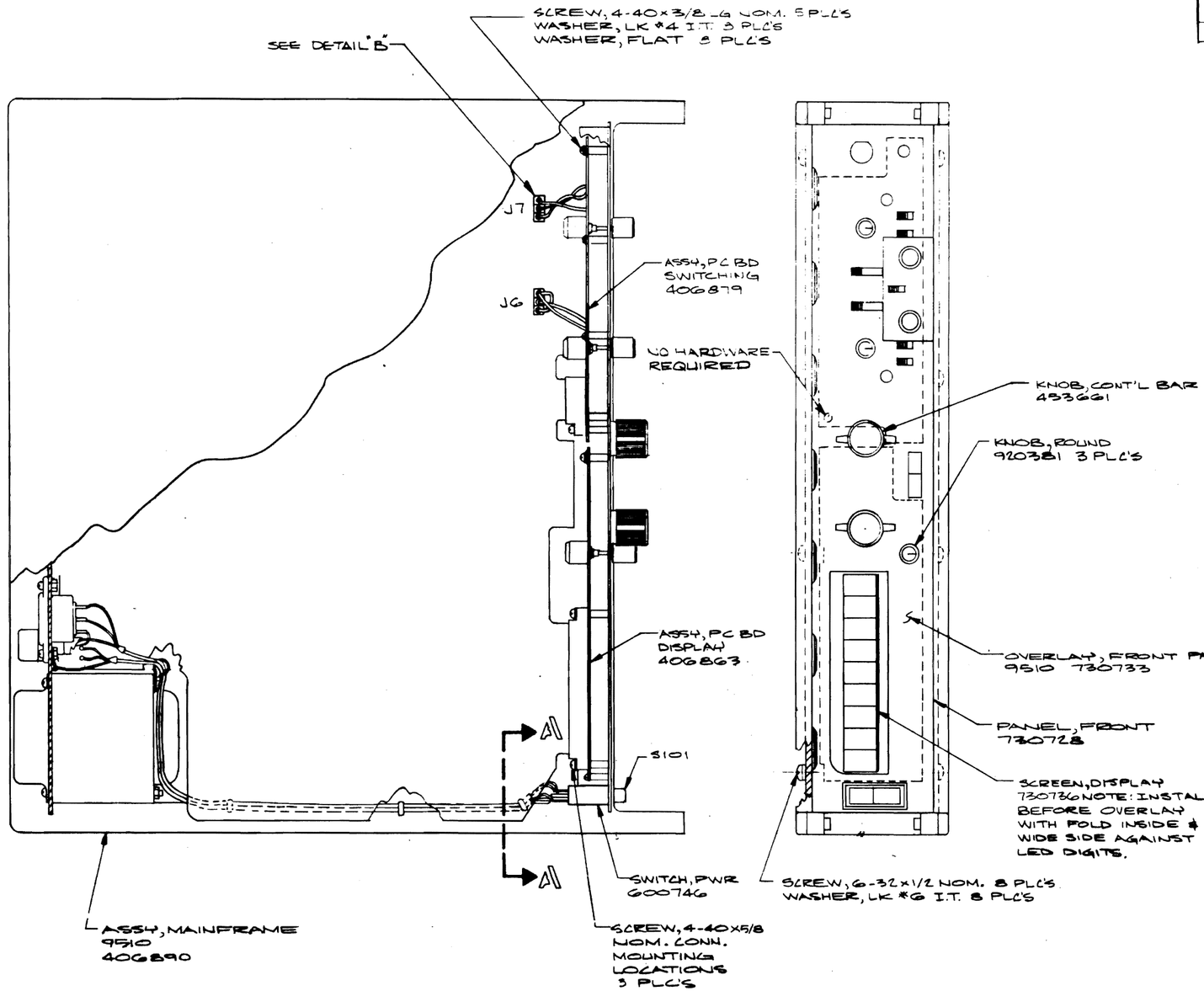
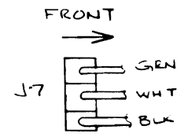
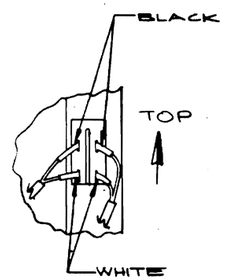
SCANS
By
Artek Media

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APP
	A	RELEASED PER DRN # 11499			
	B	REVISED PER EO # 11779			





DETAIL "B"



VIEW A1-A1
SCALE: NONE

2. PLUG CONN "J7" TO MOTHER PCB WITH BLK WIRE TOWARD CONN "J6" AS SHOWN
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	D. ENNE	10/10/77
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		11/4/77
PROD ENGR		11/7/77

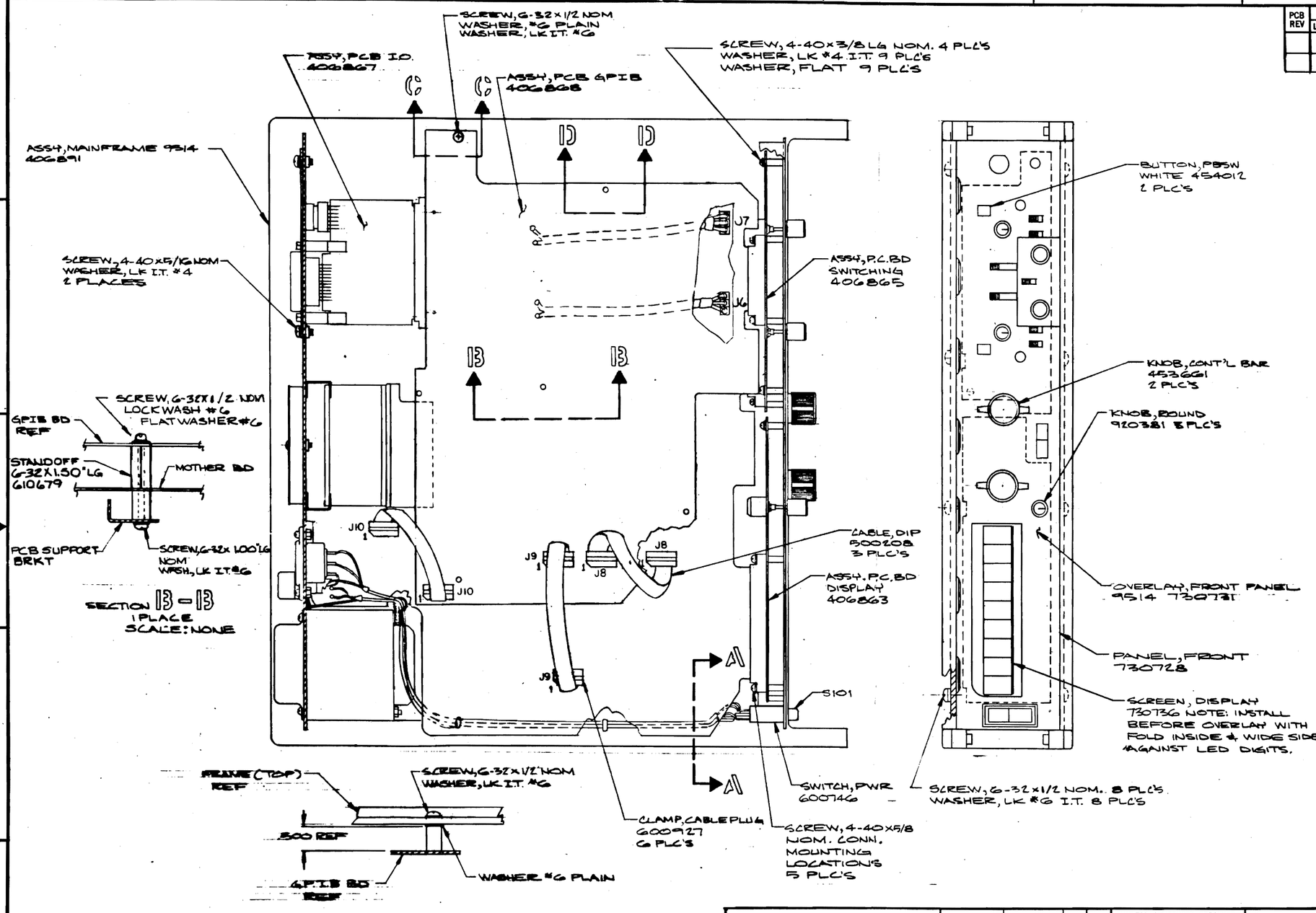
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY, CHASSIS 9510

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	40[illegible]88	E

SCALE NONE SHEET OF 2

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1149 11/7/77			
	B	REVISED PER EO 11780			



1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

406914	9514		1
NEXT DWG	USED ON	NEXT DWG	NAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	B. VENNE	10/10/77
CHECK		11/4/77
DESIGN		11-4-77
MECH ENGR		
PROJ ENGR	K. McClellan	11/4/77
PROD ENGR		11.7.77

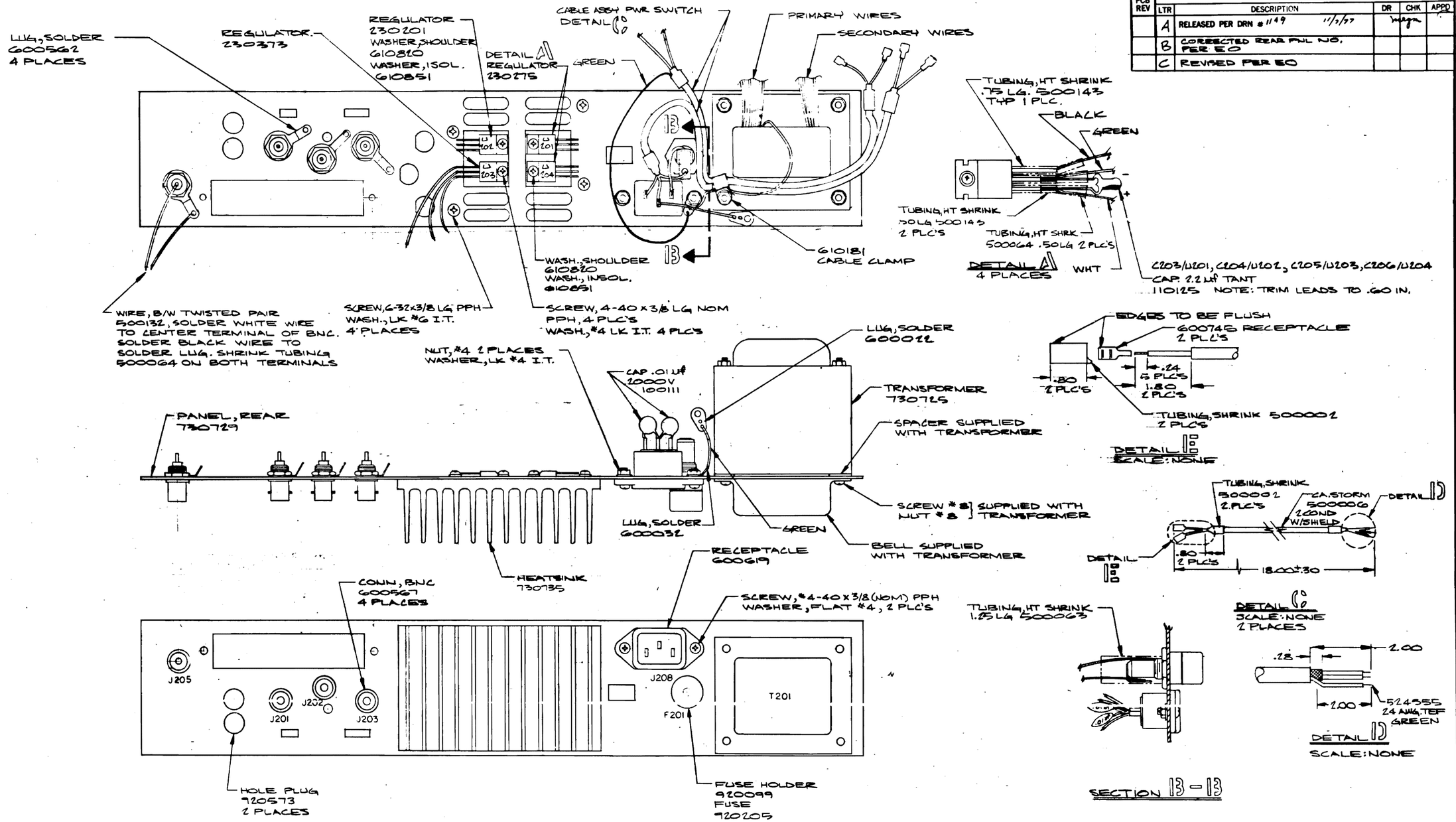
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY, CHASSIS 9514

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406889	B

SCALE NONE SHEET 1 OF 2

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1149 11/2/77	Maya		
	B	CORRECTED REAR PNL NO. PER EO			
	C	REVISED PER EO			



1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	- .004
XX.020	FORMED	- .001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

NEXT DWG	USED ON	QTY REQD
	APPLICATION	

DRAWN	[illegible]	[illegible]
CHECK	[illegible]	[illegible]
DESIGN		
MECH ENGR	[illegible]	[illegible]
PROJ ENGR	[illegible]	[illegible]
PROD ENGR	[illegible]	[illegible]

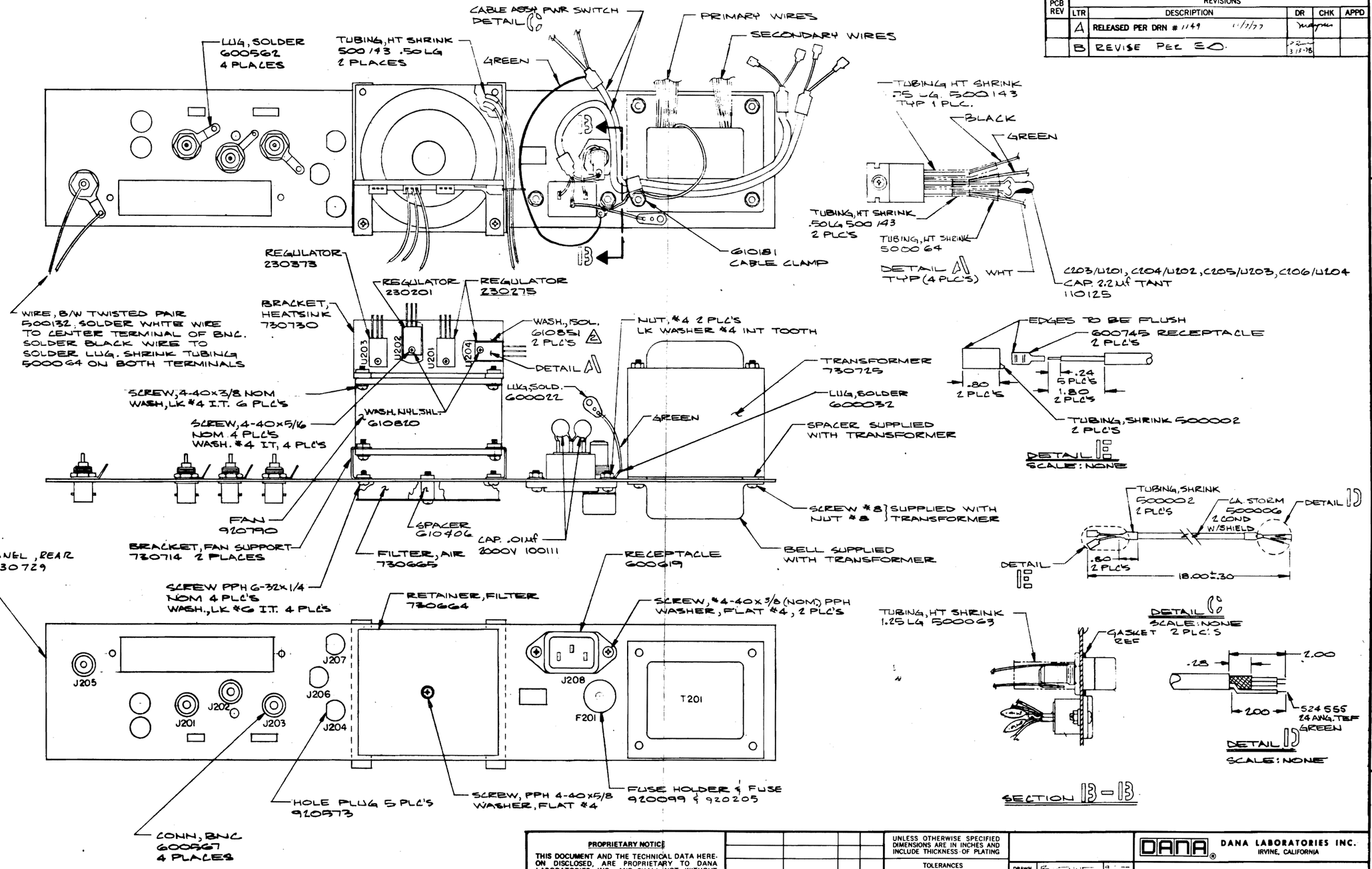
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

ASSY, REAR PANEL 9510

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	06882	C

SCALE 1=1 SHEET OF

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1149 11/2/77			
	B	REVISE PER E.O.	3/15-78		



2 USE THERMAL COMPOUND P/N 920469 ON REGULATORS U201-U204 IF ISOLATING WASHERS ARE NOT AVAILABLE.

1 ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS

NOTES: UNLESS OTHERWISE SPECIFIED

406891	95.4	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	B. RENNE	9-27-77
CHECK		11-77
DESIGN		
MECH ENGR		11-77
PROJ ENGR	K. Fitzgerald	11/7/77
PROD ENGR		11/7/77

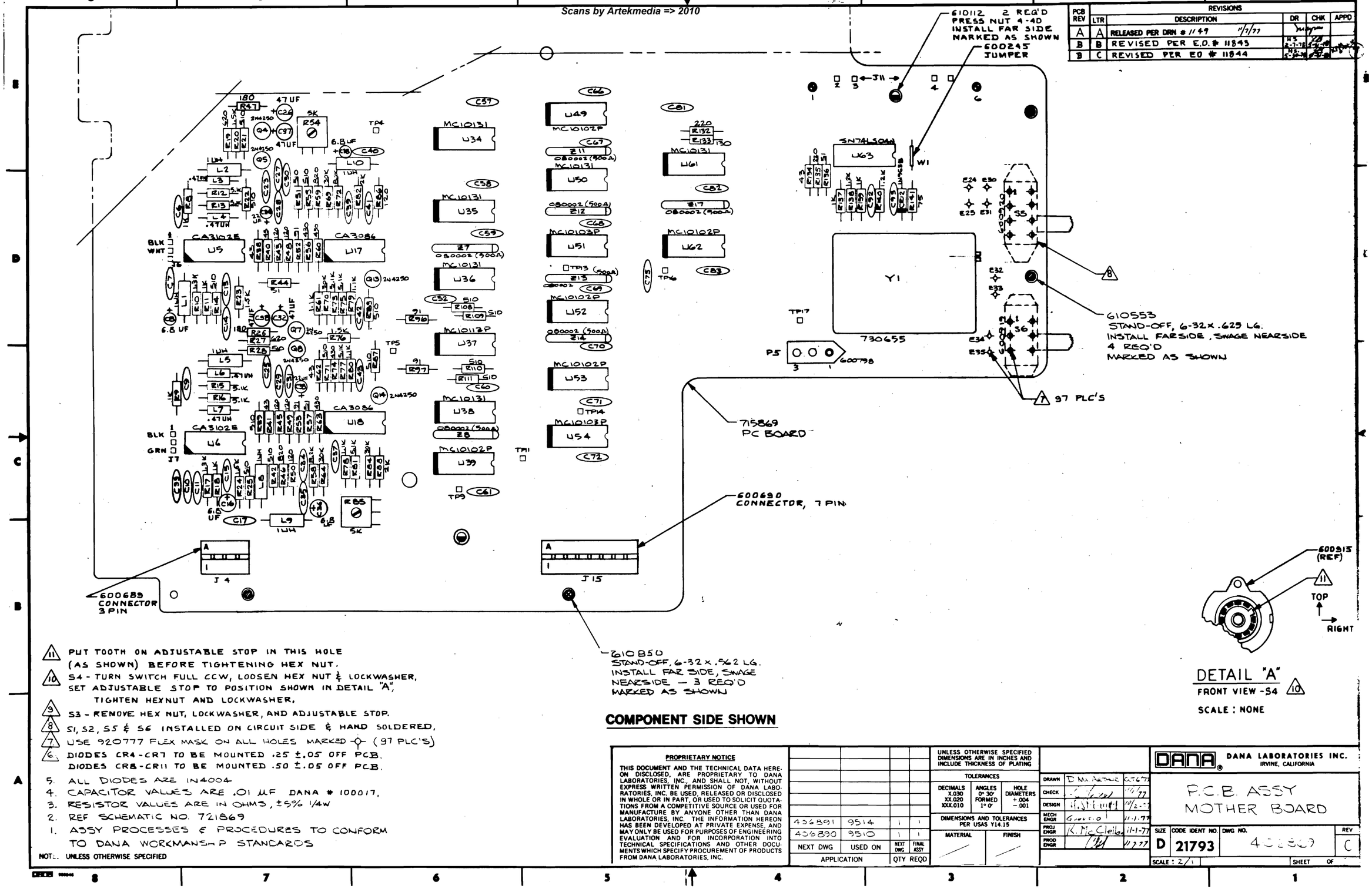
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY, REAR PANEL 9514

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406883	B

SCALE 1=1 SHEET 1 OF 1

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 11149 11/7/77			
B	B	REVISED PER E.O.# 11845	HS 2-7-78		
B	C	REVISED PER EO # 11844	HS 5-2-78		



DETAIL "A"
FRONT VIEW - S4 (10)
SCALE : NONE

(11) PUT TOOTH ON ADJUSTABLE STOP IN THIS HOLE (AS SHOWN) BEFORE TIGHTENING HEX NUT.

(10) S4 - TURN SWITCH FULL CCW, LOOSEN HEX NUT & LOCKWASHER, SET ADJUSTABLE STOP TO POSITION SHOWN IN DETAIL "A", TIGHTEN HEXNUT AND LOCKWASHER.

(9) S3 - REMOVE HEX NUT, LOCKWASHER, AND ADJUSTABLE STOP.

(8) S1, S2, S5 & S6 INSTALLED ON CIRCUIT SIDE & HAND SOLDERED.

(7) USE 920777 FLEX MASK ON ALL HOLES MARKED ⊕ (97 PLC'S)

(6) DIODES CR4-CR7 TO BE MOUNTED .25 ±.05 OFF PCB.
DIODES CR8-CR11 TO BE MOUNTED .50 ±.05 OFF PCB.

5. ALL DIODES ARE IN4004
4. CAPACITOR VALUES ARE .01 µF DANA # 100017.
3. RESISTOR VALUES ARE IN OHMS, ±5% 1/4W
2. REF SCHEMATIC NO. 721869
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS

NOTE: UNLESS OTHERWISE SPECIFIED

COMPONENT SIDE SHOWN

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406891	9514	1	1
406890	9510	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+ .004
XX.020	FORMED	- .001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	D. McArthur	10/6/77
CHECK		11/7/77
DESIGN		10/2-7
MECH ENGR		11-1-77
PROJ ENGR	K. McCleila	11-1-77
PROD ENGR		11/7/77

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

P.C.B. ASSY
MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406890	C

SCALE : 2/1 SHEET OF

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
		SEE SHT 1			

453900
POST, 4 REQ'D
MARKED AS SHOWN
INSTALL NEARSIDE

920734
SOCKET, 14 PIN
(U5, 6, 8, 17, 18, 19, 40
42, 43, 45, 55, 56, 57, 58)
14 REQ'D
MARKED AS SHOWN

500147
TUBING, SHRINK 1" ID X 3/4 L. APPROX.
(INSTALL AROUND C84 & C85)

600786
POST, 32 REQ'D
MARKED AS SHOWN
INSTALL NEAR SIDE

715869
PC BOARD
(REF)

500005
TIE CORD, NYLON
2 PLACES

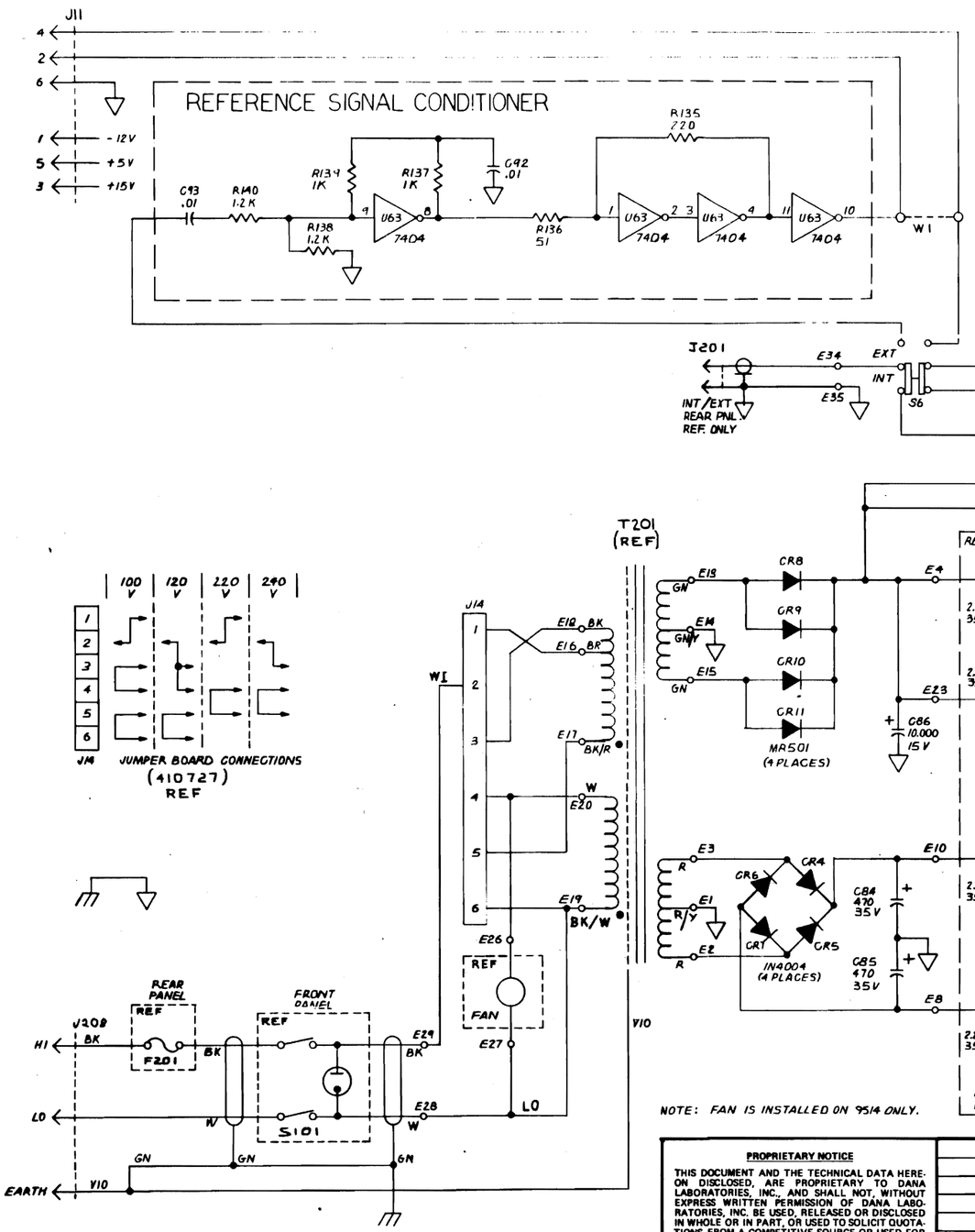
920735
SOCKET, 16 PIN
(U1, 12, 16, 26, 34, 35,
36, 37, 38, 39, 41, 49, 50,
51 52 53 54 60 61 62.
J8, 9, 10.
23 REQ'D
MARKED AS SHOWN

600823
SOCKET
40 PIN

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406869	C

SCALE: 2/1 SHEET 2 OF 9

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN #			



NOTE: FAN IS INSTALLED ON 9514 ONLY.

2. CAPACITOR VALUES ARE IN UF
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406869	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	
CHECK	
DESIGN	
MECH ENGR	
PROJ ENGR	
PROD ENGR	

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE —— SHEET 7 OF 7

PCB REV	REVISIONS LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			

SIGNAL COND A

TRIGGER DETECTOR

INPUT DISABLE

SCHMITT TRIGGER

HYSTERESIS COMP.

SIGNAL COND B

TRIGGER DETECTOR

INPUT DISABLE

SCHMITT TRIGGER

HYSTERESIS COMP.

NOTE 1
THIS CIRCUIT INVERTS SIGNAL WHEN IN NEG SLOPE.
IT ALSO DISABLES THE INPUT CHANNEL A AND B
WHEN IN CHANNEL C MEASUREMENT OPERATION

NOTES: UNLESS OTHERWISE SPECIFIED

406869	9500		
NEXT DWG	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN		
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE | SHEET 2 OF 7

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			

GPIB J8-2 J9-15 SSR RMT

START STOP REMOTE

RESET

START/STOP

FUNCTION

S3

U12 ROM 1

U16 ROM 2

S4

N RESOLUTION

GATE DELAY

S5

RESET LOGIC

GATE CONTROL SIGNAL CONDITIONER

DISPLAY TIMEOUT

GATE CONTROL REAR PNL. REF ONLY

SCRS

UPDATE

SPR

TO

MLCL

GDR

SWR

GDL

SWL

DATA READY F/F

POR

FC+RC+C/A→+CLEAR

(EXT ARM ENABLE) EAEL

(EXT ARM) EA (6E8)

GDY (GATE DELAY) (6B8)

DRES (6B8) (7A8)

CRES ATE J15-6 (5D8)

CLEAR (6D8) U24-4 (5C3) U19-13 (7D4)

CLEAR (7A8)

DRDY GPIB J8-15

S/S (6C8)

RMT J1-13

FB (6D8)

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406869	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	
CHECK	
DESIGN	
MECH ENGR	
PROJ ENGR	
PROD ENGR	

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC
MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE —— SHEET 3 OF 7

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
PCB REV	DESCRIPTION	DR	CHK	APPD
	RELEASED PER DRN #			

TIA SYNCHRONIZER

(3E6) U12-13

(3E6) B11 U12-9

(3E6) U11-8 B10 $\overline{TIA}$ 13 Z10 14

(6B1) ARM

CARM J15-2

Z1-6 10KΩ +5

U48 74LS10

U46 74LS04

U54 10103

U36 10131

Z14-2 500

Z7-7 500

Z14-6 500

Z7-3 500

4 Z6 13

FROM S.C.A. (2C4) f_a

U54 10103 N.C. 15 17 9

Z15-4 500

+15V

R125 560

Q24 2N4248

Q28 2N4248

Z15-7 500

R124 180

U39 10102 9 5 2 GOSC

MINOR TIA GATE

TP14

TP9

(3B4) Z16-3

U38 10131 N.C. 10 12 15

Z7-7 500

U38 10131 7 5 2 6 3

Z8-1 500

U39 10102 11 10 14

U54 10103 10 11 14

Z14-7 500

Z14-5 500

Z8-4 500

U54 10103 7 3 11 N.C. 6

Z8-6 500

Z8-3 500

FROM S.C.B. (2C1) f_b

U52 10102 NC 11 10 14

U39 10102 6 N.C. 3

Z7-6 500

Z8-8 500

10 MHz OSC (1E3)

U46 74LS04 13 12

GLOCK

U46 74LS04 11 10

10 Z10 7

TP8

U11 74LS02 9 8 10

10 Z6 7

CHK (2A8)

TEST

D2-5 (2D5) (2D1)

U53 10102 12 9 15

Z15-8 500

+15

R122 560

Q26 2N4248

Q22 2N4248

Z15-2 500

R128 180

R120 180

CHANNEL A

ECL TO TTL CONVERTERS

CHANNEL B

U39 10102 15 9

Z15-3 500

+15V

R130 560

Q23 2N4248

Q27 2N4248

Z15-6 500

R118 180

R117 180

MARKER GENERATOR

+5V

U59 V2 74LS74 10 12 9 11 8 13

R116 49

E24

J1205

E25

MARKER OUT REAR PNL. REF. ONLY

+5V

U59 V2 74LS74 4 2 6 3 1

$\overline{TIA}$ (6B8)

GOSC (5E8)

f_a (ECL) (5E8)

$\overline{f_a}$ (TTL) (6C8)

f_a (TTL) (5B8)

$\overline{f_b}$ (TTL) (6C8)

f_b (ECL) (5E8)

f_a (TTL) (5D8)

NOTES: UNLESS OTHERWISE SPECIFIED

406869	9500		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN			
CHECK			
DESIGN			
MECH ENGR			
PROJ ENGR			
PROD ENGR			

DANA® DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC

MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE — SHEET 4 OF 7

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			

ACCUMULATOR INPUT LOGIC

GOSC (4E1)
B5 (3D6)
BB (3D6)
FB (ECL) (4B1)
B7 (3D6)
FF (TTL) (4B1)
ATE (3B1)
(6B8) U26-13
(6D1)
FF (ECL) (4B1)
RA (3C8)
RB (3C8)
RC (3C8)
U15-4
A=B (4E1)
B2 (6C7) U26-1
B6 (3B4)
(4D1)
B3 (3D6)

U53 10102 · U52 10102 · U51 10103 · U51 10109 · U52 10102 · U32 74LS00 · U46 74LS04 · U33 74LS00 · U45 74LS90 · U44 74LS00 · U48 74LS10 · U30 74LS00 · U14 7405 · U21 74LS74 · U29 74LS04

Z13-6 500 · Z14-3 500 · Z14-4 500 · Z13-8 500 · Z13-2 500 · Z13-7 500 · Z13-4 500 · Z12-3 500 · Z19-5 500 · Z12-5 500 · Z14-2 10K · Z14-5 10K

MEASUREMENT SIGNAL · MAJOR (MEASUREMENT) GATE · TP13 · TP16 · TP12 · N.C.

GATE

TIMEBASE COUNTER CONTROL

AUTO TRIGGER LATCHES

R107 500 · R114 560 · R103 2K · Z7-8 500 · Z9-7 500 · R68 510 · Z9-6 500 · Q12 2N4248 · U35 10131 · U52 10102 · U50-13 (7B8)

Q19 2N4258 · R106 100 · R105 360 · Z9-8 500 · U47 74LS02

$\overline{SXL}$ → J10-13 · $\overline{SLVL}$ → J10-5

TIMEBASE COUNTER

TIMEBASE SYNC F/F'S

U41 74LS151 · U24 74LS74 · U35 10131 · U25 74LS04 · R102 10K · Z7-9 500 · (6B6) U62-6, 11 · U22-3 (3C1)

(6B4) U30-8

U40 · U42 · U43 · U58 · U57 · U56 · U55 74LS90

NOTES: UNLESS OTHERWISE SPECIFIED

406869	9500
NEXT DWG	USED ON
APPLICATION	QTY REQD

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN · CHECK · DESIGN · MECH ENGR · PROJ ENGR · PROD ENGR

DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC
MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE — · SHEET 5 OF 7

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			

EXTERNAL ARMING LOGIC

MEASUREMENT GATE INPUT CONTROL

MAJOR GATE LOGIC

END OF GATE

GPIB J9-11 EAER
EAEL (3A1) EAEL
EA (3B1)
CLEAR (3C1) CLEAR
FB (3C1)
B9 (3D5)
TO + C/A + B4
FA(TTL)(4D1)
S/S (3E1)
FB(TTL)(4B1)
BØ (3D6)
B1 (3B6)
B2 (3D5) FA + FC + FB
MLCL (3B8)
(5D8) U41-5 TB
(5C2) U35-15
GDY (2B1)
GPIB J8-13 UPDR
DRES (3D1)
TO (3C8)
GATE (5D8)
ARM (6D8)
UPDATE (3C8)
START
STOP
LOAD
TP1D
TP2
U41-4 (7B4)
U40-6 (5B4)
U21-13 (5B4)
U14-13 (7B4)
J1-D
J1-B
J202
GATE OUT REAR PNL REF. ONLY

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406869	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN		
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
MOTHER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE — SHEET 6 OF 7

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			

(9B6) DPB1
(3B6) DPB2
(8B6) DPB3

(9E6) B11
J15-5
J15-F
J15-7
J15-4
J15-8 fc/10

(6C6) U4-4

U7p9 STA J8 → 3
U8p7 STB → 5
U8p5 STC → 6
U8p3 STD → 7
C/A→B +TO → J1-C

2N 4248 Q11 Q15 4248 Q16 4248
R66 100 R65 100 R67 100
R36 360 R35 360 R95 360
U60 LS157
Z5=5K

2ND DIGIT
6 DIGITS
Z5 R=5K
R89 5K
CR17 1N960
Z4-3 10K
U19 79196
GLEAR (SC1)
R5 2.2K C3 .01 R30 2.2K
U2 L904
RESET
LOAD
30pF C20
OSC
SCAN
SCAN RESET
DB OUT
DB IN
BLANK

DECIMAL PT STROBE
STROBE
U1 74C151
R4 220 STDP → J1-9
L904

LSD
DIGIT STROBE
MSD
S1 S2 S3 S4 S5 S6 S7 S8

DIGIT STROBES
LS367 U3
STA → N
STB → V
STC → U
STD → P

BCD OUT A B C D
BCD CODE
Q1 2N2200 +5V
R2 220 → OF → A
R1 220 → RBI → M
SRBI → S

MOST SIGNIFICANT DIGIT
Q6 2N2200
R29 220
U8 74LS90
U7 74LS75
U23 LS02
BLANKING
U1A 7405
5K Z3-3 +5
15
18
17
16

D9 A → J9-4
D9 B → J9-9
D9 C → J9-7
D9 D → J9-6
OF → J9-K
TO GP1B

LSB ACCUMULATOR
U99 10102
U34 10131 B
U50 10131 A
R193 130 +5.2
R144 390 +15
R132 220
Q21 Q20 4258
R115 75
R145 2K
Z9-4 500
Z3-3 500
Z12-6 500
Z12-2 500
Z11-6 500
Z11-7 500
Z12-8 500
Z12-7 500
Z11-3 500
Z12-4 500
Z11-5 500
(SE1) B52-2
(SE2)
GLEAR (ECL)

CLEAR
(6B2) U11-13
JB-1 GP1B SCAN
JB-14 GP1B SCR5
J1-L RBO
(5C1) CLEAR
(3D1) DRES

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406869	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	
CHECK	
DESIGN	
MECH ENGR	
PROJ ENGR	
PROD ENGR	

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

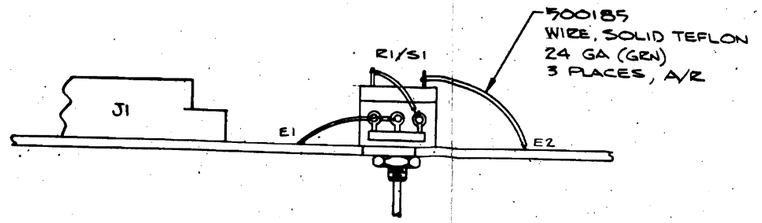
SCHEMATIC
MOTHER BOARD

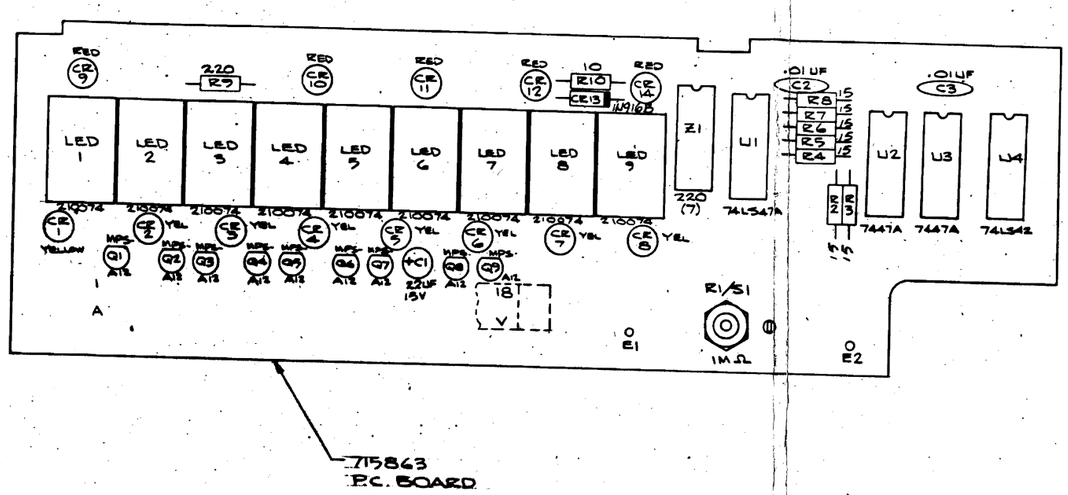
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721869	A

SCALE —— SHEET 7 OF 7

3-15

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1149 11/7/77			





1. RESISTORS ARE IN OHMS, ±5%, 1/4W
2. REF SCHEMATIC NO. 721863
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG.	FINAL ASSY
406889	9514	1	
406888	9510	1	
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	D. MacKenzie	10/3/77
CHECK		11/1/77
DESIGN		
MECH ENGR	G. Iacocca	11-1-77
PROJ ENGR	K. McClellan	11-1-77
PROD ENGR		11-7-77

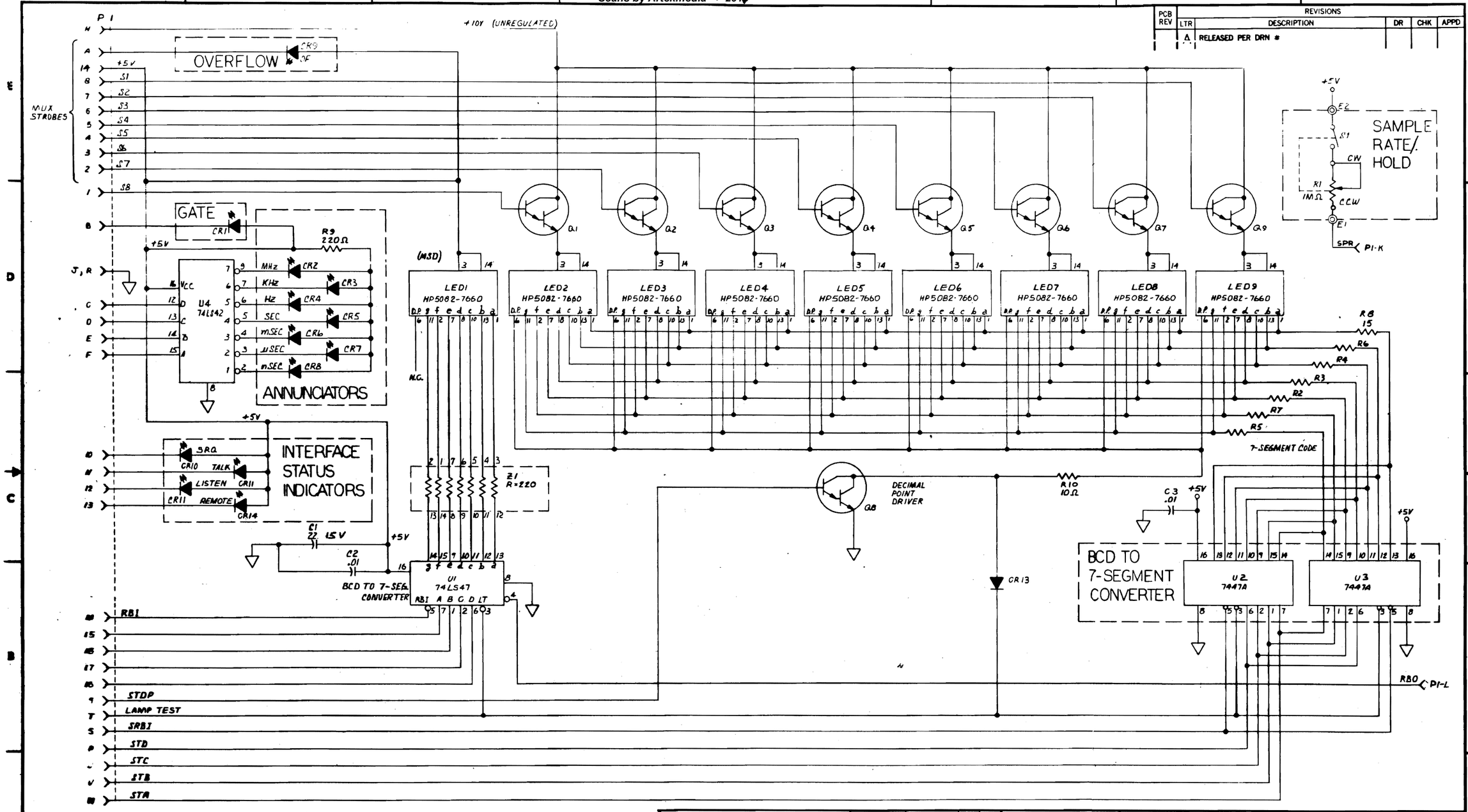
DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C.B. ASSY DISPLAY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406863	A

SCALE: 2/1 SHEET 1 OF 3

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN #			



4. RESISTORS R2 THRU R8 ARE 15 OHMS
3. TRANSISTORS ARE MPS-A12
2. CAPACITOR VALUES ARE IN µF
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406863	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	H. Shirley	4/26/79
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

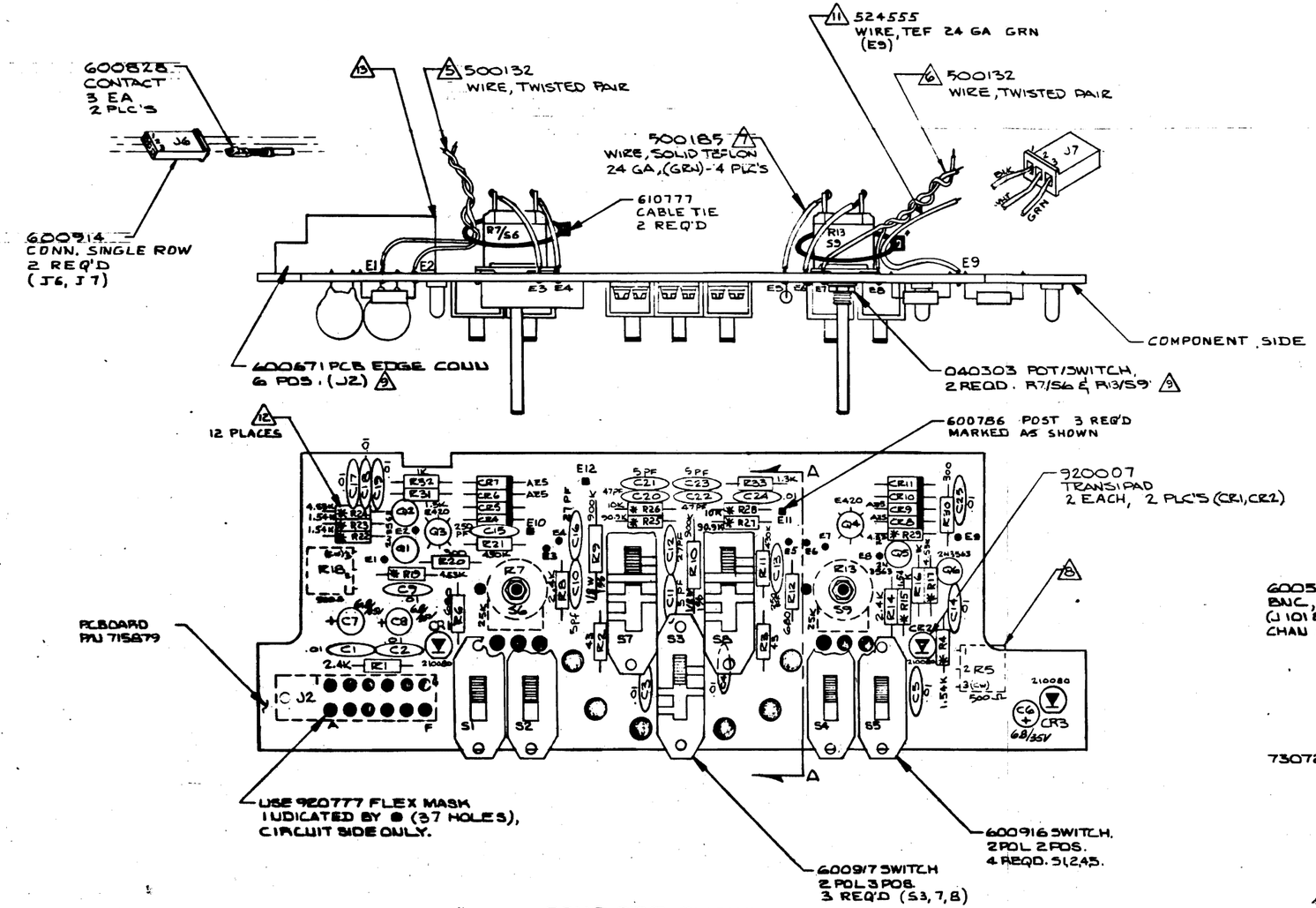
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC - 9500
DISPLAY PCB

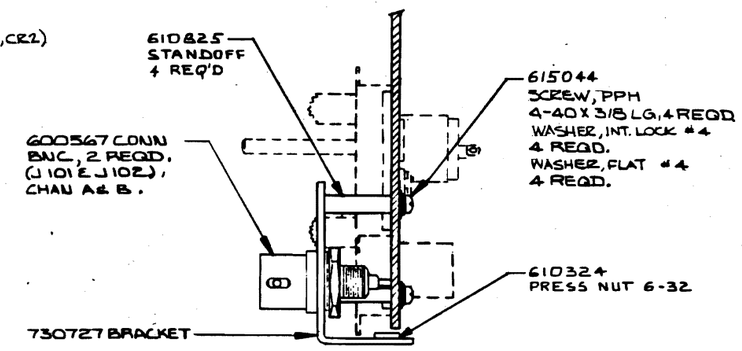
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721863	A

SCALE | SHEET 1 OF 1

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1149 11/7/77			
B	B	REVISED PER EO #	HS 2/24-78		



COMP SIDE SHOWN



SECTION A-A
"NO SCALE"
NOTE: B.N.C 600567 & MTG BRKT ARE NOT SHOWN IN OTHER VIEWS FOR CLARITY.

1. DIODES ARE 007
2. INDICATES COMPONENTS INSTALLED ON CIRCUIT SIDE & HAND SOLDERED
3. E5 AND E8 MOUNTED ON REAR SIDE AS SHOWN WITH ADJ. SCREW FACING OUT OR AWAY FROM BOARD
4. KEEP WIRES AS SHORT AS POSSIBLE
5. E7 TIES TO J7 POS 1 WITH BLACK WIRE AND E8 TIES TO J7, POS 2 WITH WHITE WIRE OF TWISTED PAIR. TOTAL LENGTH OF WIRE TO BE 2 1/4 IN ± 1/4 IN.
6. E1 TIES TO J6, POS. 2 WITH WHITE WIRE AND E2 TIES TO J6, POS 1 & 3 WITH BLACK WIRE OF TWISTED PAIR. TOTAL LENGTH OF WIRE TO BE 3 IN. ± 1/4 IN.
7. CAPACITOR VALUES ARE IN μF,
8. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
9. REF SCHEMATIC NO. 721879
10. ASSY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS

△10 CUT-OFF EDGE CONN. J2 AS SHOWN
△11 * INDICATES RESISTORS ARE 1/10W ± 1%
△H E8 TIES TO J7 POS 3 WITH GREEN WIRE TOTAL LENGTH OF WIRE TO BE 2 1/2 IN ± 1/4 IN.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406895	35:10		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	J. MacArthur	OCT 5 '77
CHECK		11/1/77
DESIGN		
MECH ENGR	Guercia	11-1-77
PROJ ENGR	K. McClellan	11-1-77
PROD ENGR		11-7-77

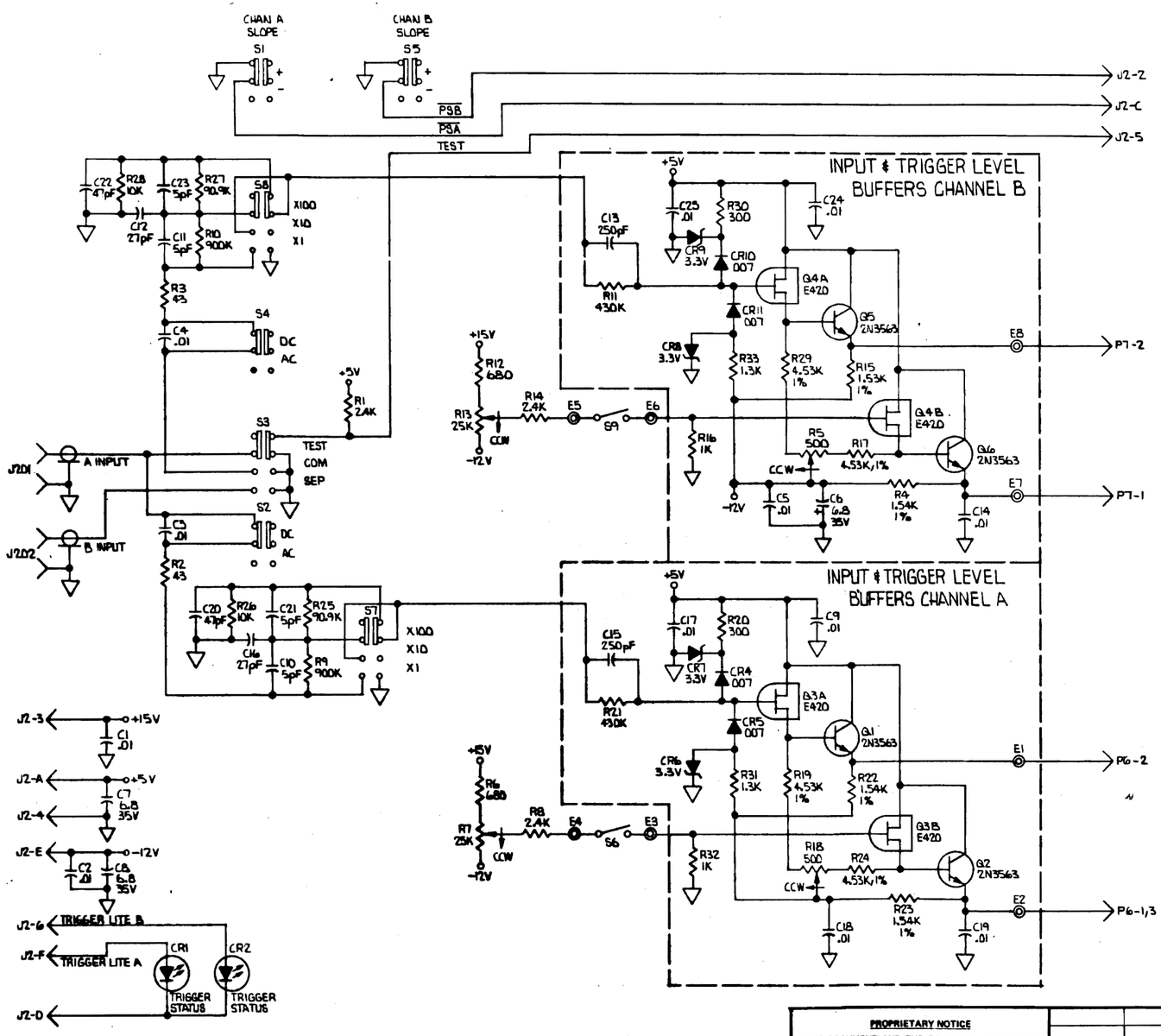
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

P.C.B. ASSY SWITCHING

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406879	B

SCALE 2:1 SHEET 1 OF 4

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APVD
		RELEASED PER DRN #			



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS.
2. ALL CAPACITORS ARE IN μF.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406879	9510		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	J. Benson	4/24/78
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

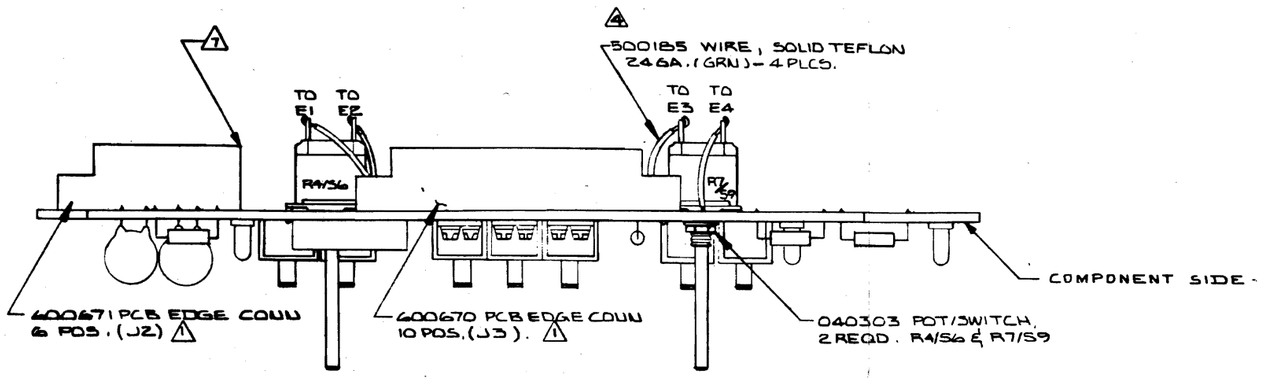
DANA LABORATORIES INC. IRVINE, CALIFORNIA

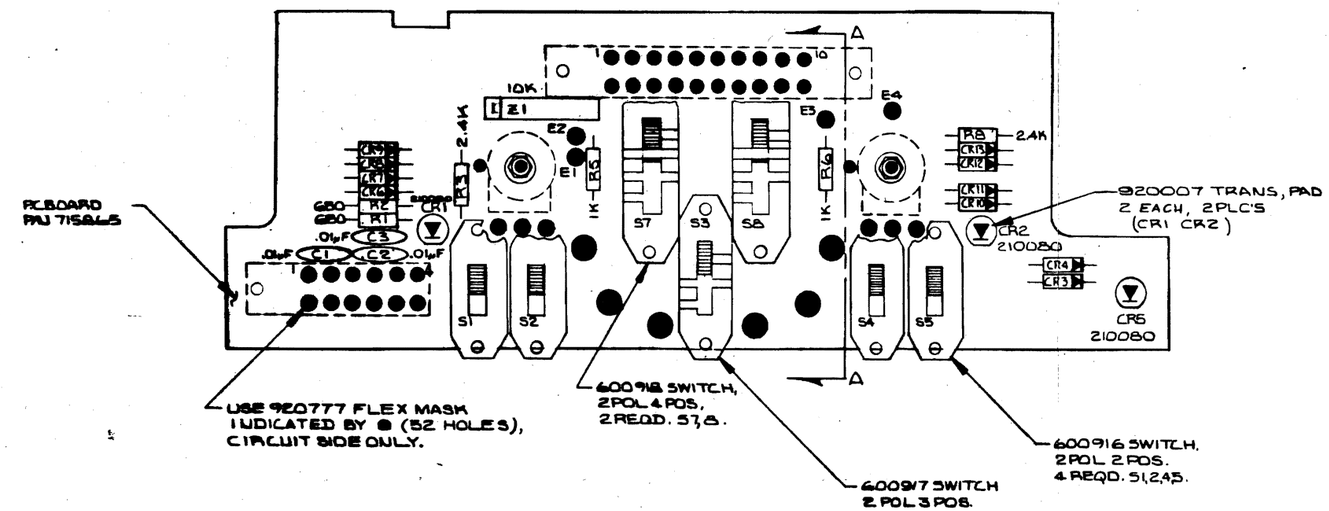
SCHEMATIC— MODEL 9510 SWITCHING PRINTED CIRCUIT BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721879	A

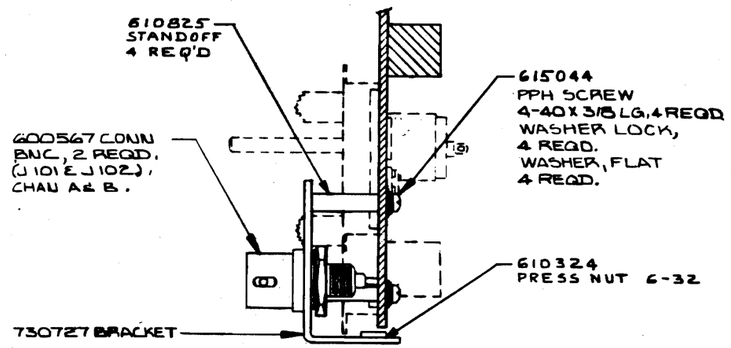
SCALE NONE | SHEET 1 OF 1

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
B	A	RELEASED PER DRN # 1149 11/7/77		mayo	
C	B	REVISED PER E.O.#	HS 2-28-78		





COMP SIDE SHOWN



SECTION A-A
"NO SCALE"
NOTE: B.N.C 600567 & MTG BRKT ARE NOT SHOWN IN OTHER VIEWS FOR CLARITY.

1. CUT-OFF EDGE CONN. J2 AS SHOWN
6. ALL DIODES ARE IN916B; CR3-CR4, CR6-CR15
5. REF. SCHEMATIC 721865
4. KEEP WIRE AS SHORT POSSIBLE
3. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, ±.5% CC
1. INDICATES COMP. INSTALLED ON CIRCUIT SIDE & HAND SOLDERED.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406890	9514		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Byung	9-6-77
CHECK		11/11/77
DESIGN		
MECH ENGR	Guerrero	11-1-77
PROJ ENGR	K. McClellan	11-1-77
PROD ENGR		11-11-77

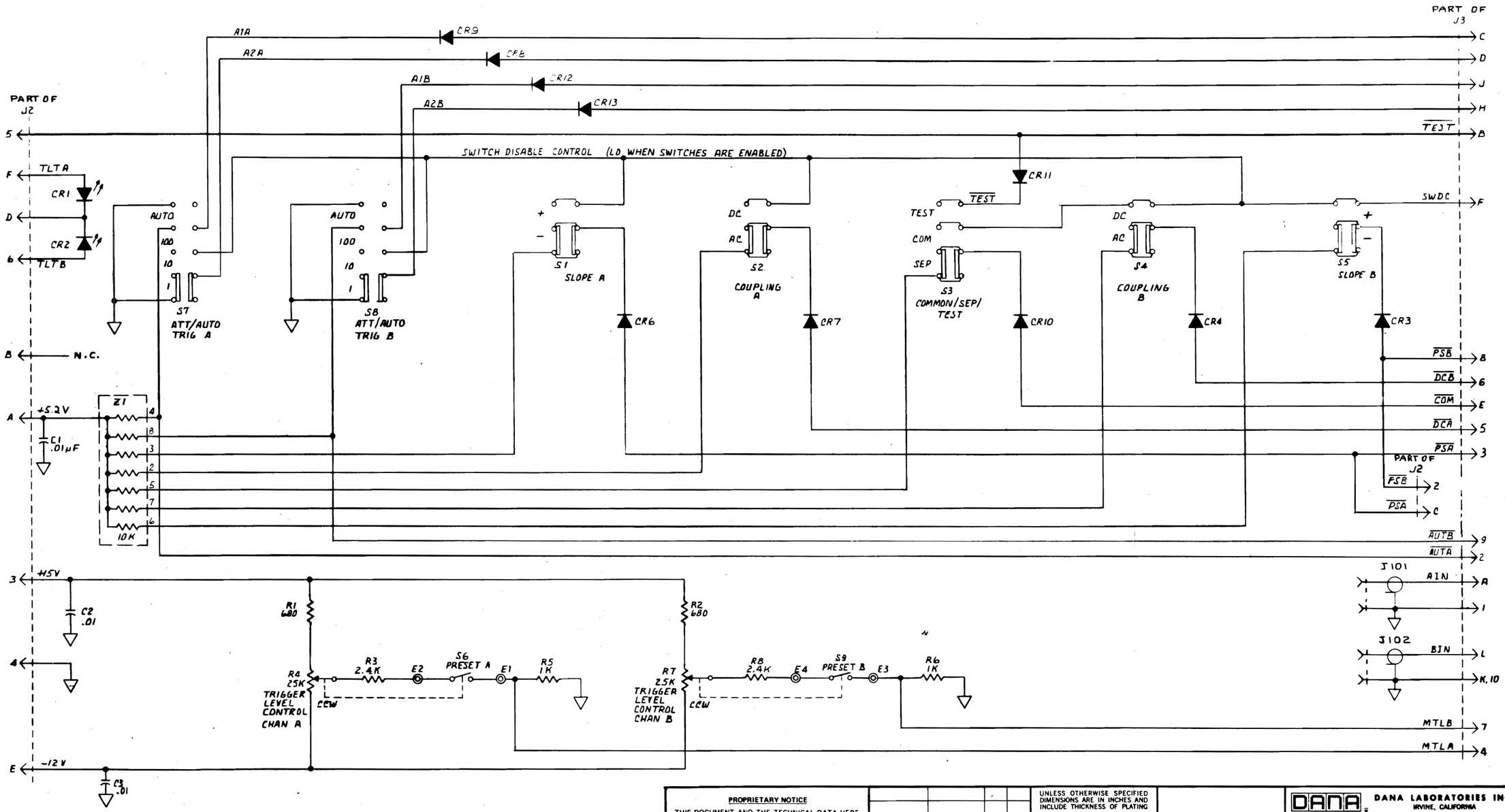
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY - P.C. BOARD SWITCHING

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406865	B

SCALE 2/1 SHEET 1 OF 3

P.C.B. REV	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN #			



4. LED's ARE HP4082-4655
3. DIODES ARE IN916B
2. CAPACITOR VALUES ARE IN μF
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406865	9514		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+ .004 − .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	H. Stolz	7/24-76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC - MODEL 9514 SWITCHING PCB

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	721865	A

SCALE —— SHEET 1 OF 1

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SCANS
By
Artek Media

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1130 11/10/77	[illegible]		
B	B	REVISED PER EO #	MS 2-1-78		

600823 SOCKET 40 PIN
920624 SOCKET 24 PIN
920734 SOCKET 14 PIN 12 REQ'D MARKED AS SHOWN
920735 SOCKET, 16 PIN 25 REQ'D MARKED AS SHOWN
600245 JUMPER WIRE 2 REQ'D
920585 CUP 453539 BUMPER 610487 STRAP
920777 FLEX MASK 49 PLC'S MARKED AS SHOWN
600926 SWITCH 2 REQ'D INSTALLED ON CIRCUIT SIDE
610336 STAND-OFF 6-32 x 1/2 LG. INSTALL NEARSIDE SWAGE FARSIDE
715868 P.C. BOARD
600766 EYELET, 4 REQ'D
600786 POST, 13 REQ'D MARKED AS SHOWN INSTALL NEAR SIDE
600933 HEATSINK
610533 PRESSNUT 6-32 FARSIDE P.C.B. SCREW 6-32 LOCKWASHER
230275 REGULATOR, 920469 M.S. COMPOUND BETWEEN U45 AND BOTH HEATSINKS
600932 HEATSINK
SEE DETAIL "A"
SEE DETAIL "B"
500227 CONNECTOR

COMPONENT SIDE SHOWN

DETAIL "A"
SCALE: NONE

501446 CABLE COAX 2 REQ'D
J6,7 E1,2 E3,4

DETAIL "B"
TYP 2 REQ'D SCALE: NONE

600914 HOUSING 2 REQ'D
600828 CONTACT 2 EACH 2 PLC'S (PIN 1 & 2)
COMPONENT SIDE OF PCB
CENTER CONDUCTOR
524000 WIRE BLK .9 BEFORE STRIPPING
500001 1.0 LG. TUBING
500001 .5 LG. TUBING
BRAIDED SHIELD
501446 CABLE, COAX (REF)
WIRE WHT 524999 .7 BEFORE STRIPPING

7. INSTALL AFTER WAVE SOLDER AND CLEANING
6. * INDICATES RESISTORS ARE 1/10 W, ± 1%
5. ALL DIODES ARE IN3163
4. CAPACITOR VALUES ARE .01 μf 100V
3. RESISTORS ARE IN OHMS, ± 5%, 1/4 W
2. REF. SCHEMATIC NO. 721868
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTE: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406869	9514	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	± .004
XX.020	FORMED	± .001
XXX.010	1° 0°	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	[illegible]	11/8-77
CHECK	[illegible]	11/8-77
DESIGN	[illegible]	11/8-77
MECH ENGR	G. McCLU	11-15-77
PROJ ENGR	K. McClellan	11/15/77
PROD ENGR	[illegible]	11/8/77

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSEMBLY — IEEE-488/1975 INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406868	B

SCALE 2/1 SHEET 1 OF 8

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
B	A	RELEASED PER DRN #			

J10-13 STL
J10-5 SLVL
J11-6 TON
J11-9 AD5
J11-U AD4
J11-V AD3
J11-17 AD2
J11-18 AD1

SXL (2B7)

(2C5) ADDRESS BUS

(2E4) Φ2

HATN (2C4)
DRDY (2B5)

DATA BUS (2E6)

74LS367

J8-15 DRDY
J9-16 OF
J8-7 STD
J8-6 STC
J8-5 STB
J8-3 STA

U16-1,15 → SD

J11-B HDAVI
J11-A LRFDI
J11-C LDACI
J11-R HATN
J11-P NREN (2C8)
J8-9 RTL
(3A2) SRA
(3A2) SRB

U35-1 → S3

U41-1

J11-13 HIFC → U23 74LS04
J11-7 DI7
J11-4 DI6
J11-5 DI5
J11-6 DI4
J11-2 DI3
J11-1 DI2
J11-3 DI1

U34-1,15 → S2

LIFC (2C8)

SXL
SLVL
TON
AD5
AD4
AD3
AD2
AD1

U41-15 → SI

U38-1,15

(2B5) ATD

FD
FC
FB
RC
RB
RA

U14-1,15 → SE

FA
D9D
D9C
D9B
D9A

U21-1,15 → S6

INPUT BUFFERS

A0
A1
A2
VMA
A7
A15
A6

U19 74LS10
U46 74LS04
U17 74LS138 → SE SD SC SB SA S9 S8 S7A

U14 74LS138 → S7 S6 S5 S4 S3 S2 S1 S0

I/O DECODER

I/O STROBES (2C9)
S8 (6D8)
S9 (6A8)
SA (3E8)
SB (3C8)

CONTROL MEMORY

+5V

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A15

U22 ROM → D7 D6 D5 D4 D3 D2 D1 D0

DATA BUS (2E6)

NOTES: UNLESS OTHERWISE SPECIFIED

ArtekMedia

406868	9514		
NEXT DWG	USED ON	NEXT DWG	FIRM ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	H. Shelupa	4/24-78
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC
IEEE
488-1975 INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721868	A

SCALE — SHEET 1 OF 6

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHT 1			

CLOCK DIVIDER

10 MHz ÷3 CLOCK

+5V, R73 3.9K, 10 MHz, J8-16, U42, U42, 74LS74, TP7

POWER UP RESET

R75 10KΩ, +5V, CR21, C70 6.8/35V, -12V

(1B6) LIFC

(1C8) HREN

MICRO PROCESSOR

(1C1) (1E4) DATA BUS

+5V, 8,2,35,36,3

CLOCK 38, RESET 40, NMI 6, IRQ 4, VMA 5, A0 9, A1 10, A2 11, A3 12, A4 13, A5 14, A6 15, A7 16, A8 17, A9 18, A10 19, A11 20, A15 25

U33 MC6802

TP8, 37 Φ2, 1,21

26 D7, 27 D6, 28 D5, 29 D4, 30 D3, 31 D2, 32 D1, 33 D0

ADDRESS BUS (1E4)

DISPLAY SCAN GENERATOR

+5V, U44 74LS74, U40 74LS93, TP4, 2,3, 6,7,10

(1E5) $\overline{SXL}$

AUTO TRIGGER TIME OUT F/F

R74 10K, +5V, C62 1/35V, U43 74LS123, (ONE SHOT)

S7A

(1E6) DRDY

ATO (1B6)

BUS BUFFER

Φ2 (1E3)

74LS04

D7 U29 $\overline{D7}$, D6 U29 $\overline{D6}$, D5 U29 $\overline{D5}$, D4 U29 $\overline{D4}$, D3 U26 $\overline{D3}$, D2 U26 $\overline{D2}$, D1 U26 $\overline{D1}$, D0 U26 $\overline{D0}$

(1E6) HATN

(1C1) I/O STROBES

COUNTER LOGIC RESET

+5V, R72 10K, R71 10K, C53 1/35V, U32 74LS123, U46 74LS04, TP5, +5V

S7A

S5R, SD J8-2

$\overline{D0}$

S5

S4

S7

S6

U27 74LS174: $\overline{D5}$ $\overline{D4}$ $\overline{D3}$ $\overline{D2}$ $\overline{D1}$ $\overline{D0}$

U38 74LS175: $\overline{D7}$ $\overline{D6}$ $\overline{D5}$ $\overline{D4}$ → D07 J11-M, D06 J11-K, D05 J11-J

U36 74LS175: $\overline{D3}$ $\overline{D2}$ $\overline{D1}$ $\overline{D0}$ → D04 J11-L, D03 J11-E, D02 J11-F, D01 J11-H

U28 74LS175: $\overline{D3}$ $\overline{D2}$ $\overline{D1}$ $\overline{D0}$

U23 74LS174: D5 D4 D3 D2 D1 D0

OUTPUT LATCHES

$\overline{D0}$ (6DB)

$\overline{D0}$ (3E8)

HLZ (4B8)

(5A7)

U25 74LS00, U46 74LS04 → END J11-8

U25 74LS00, U29 → HDAY0 J11-10

LRFD0 J11-11

U25 74LS00 → LDAC0 J11-9

U25 74LS00, U19 74LS10 → L DEN J11-15

R69 220: TALK J9-13, LISTEN J9-12, HSRQ0 R56 220 J11-D, SRQ J9-14

R57 220 → RMT J9-15, RMT (3C8)

$\overline{GDR}$ J9-8, $\overline{SWR}$ J9-2, $\overline{UPDR}$ J8-13

R68 620Ω, +5V, R70 620Ω, Q13 1N3646 → SCRS J8-14, SWDC J3-F

CNF (3B8)

$\overline{MLCL}$ J9-10

SCAN J8-1

NOTES: UNLESS OTHERWISE SPECIFIED

1. R74 IS 100K OHMS WHEN OPTION 12 IS INSTALLED
2. RESISTORS ARE IN OHMS ±5%, 1/4 W
3. CAPACITORS ARE IN UF

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406868	95:4		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN, CHECK, DESIGN, MECH ENGR, PROJ ENGR, PROD ENGR

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC
IEEE-488/1975
INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721868	A

SCALE — SHEET 2 OF 6

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHT 1			

PROGRAM REGISTER

(2E1) $\overline{DO}$
(1C1) SA

U24 74LS74 CK — +5V 10,13,14

U30 74LS164 — +5V 1,9,14

U20 74LS164 — +5V 1,9,14

U44 74LS74 CK — +5V 10,13,14

PART OF U12 74LS367
U12 A1A → J3-C
U12 A2A → J3-D

PART OF U15 74LS367
U15 A1B → J3-J
U15 A2B → J3-H

PART OF U31 74LS367
U31 $\overline{DCA}$ → J3-5
U31 $\overline{DCB}$ → J3-6
U31 $\overline{PSA}$ → J3-3
U31 $\overline{PSB}$ → J3-8
U31 $\overline{COM}$ → J3-E

PART OF U12 74LS367
U12 FA → J8-10
U12 FB → J8-11
U15 FC → J8-12
U15 FD → J8-4
U15 RA → J9-1
U15 RB → J9-3
U12 RC → J9-5
U12 $\overline{EAER}$ → J9-11

PART OF U31 74LS367
U31 $\overline{TEST}$ → J3-8 → (5C7)

PROGRAM BUFFERS

DE-BOUNCE F/F'S

J3-2 AUTA — S1 — U1 74LS00 — +5V Z1 10K
J3-9 AUTB — S2 — U1 74LS00 — +5V Z1 10K

(2C1) $\overline{AMT}$
(1C1) SB

U2 74LS00 → 7405 U5
U2 74LS00 → 7405 U5

+5V Z1 10K ×2

ANALOG TRIGGER LEVEL DEMUX

+5V 16
PART OF U13 CD4053
6,8,9
10KΩ R37 +5V
CR14 A25 -12V

TP1 TP9 TP10
J10-1,8,9,16 → J11-N
J10-6,14 → -12V
C68 6.8 35V + C69 .01

TP6
(2B1) CNF

J10-7,15 → +5.2V
C64 6.8 35V + C58 .01

J10-3,11 → +15V
C60 6.8 35V + C57 .01

J10-2,4,10,12

5 VOLT REGULATOR
U45 7805
C71 6.8 35V + C63 6.8 35V + CR22 IN4005 + .01
TP11 +5V
→ J11-14

SRA (1C8)
SRB (1C8)

⚠ DECOUPLING CAPACITORS ARE: C29, 35, 40, C44, 45, 46, 47, 48, 49, 51, 52, 54, 55, 56, 59, 61, 65, 66, 67

NOTES: UNLESS OTHERWISE SPECIFIED

406868	9514		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	
CHECK	
DESIGN	
MECH ENGR	
PROJ ENGR	
PROD ENGR	

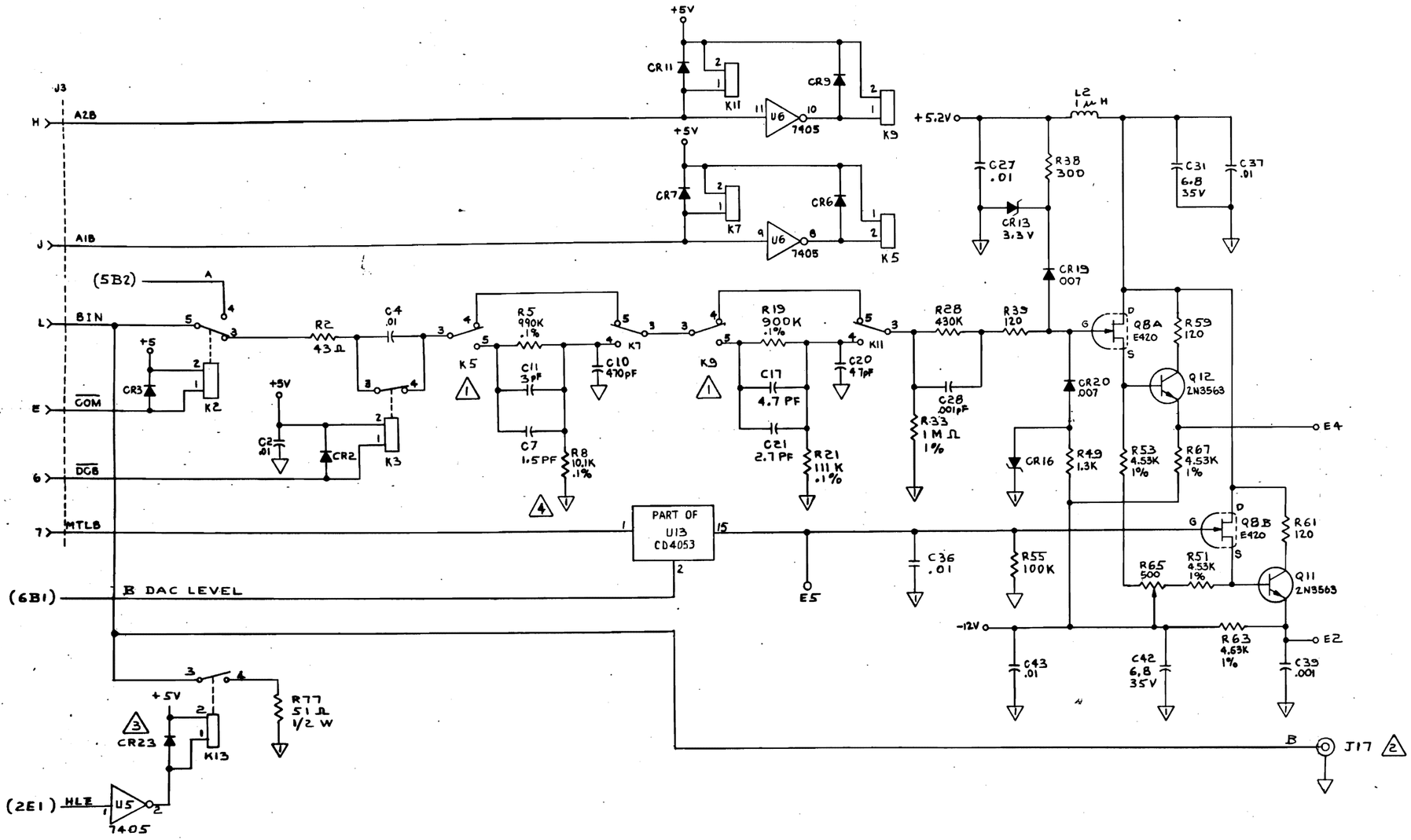
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
IEEE-488/1975
INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721868	A

SCALE — SHEET 3 OF 6

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHT 1			



△4 THE SYMBOL ▽ DENOTES SIGNAL CONDITIONER AND DAC GROUND.

△3 R77, K13 AND CR23 INSTALLED WITH OPTION 55E.

△2 J17 INSTALLED WITH OPTION 01.

△1 RELAYS SHOWN IN ENERGIZED STATE

NOTES: UNLESS OTHERWISE SPECIFIED

406868	9514		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	
CHECK	
DESIGN	
MECH ENGR	
PROJ ENGR	
PROD ENGR	

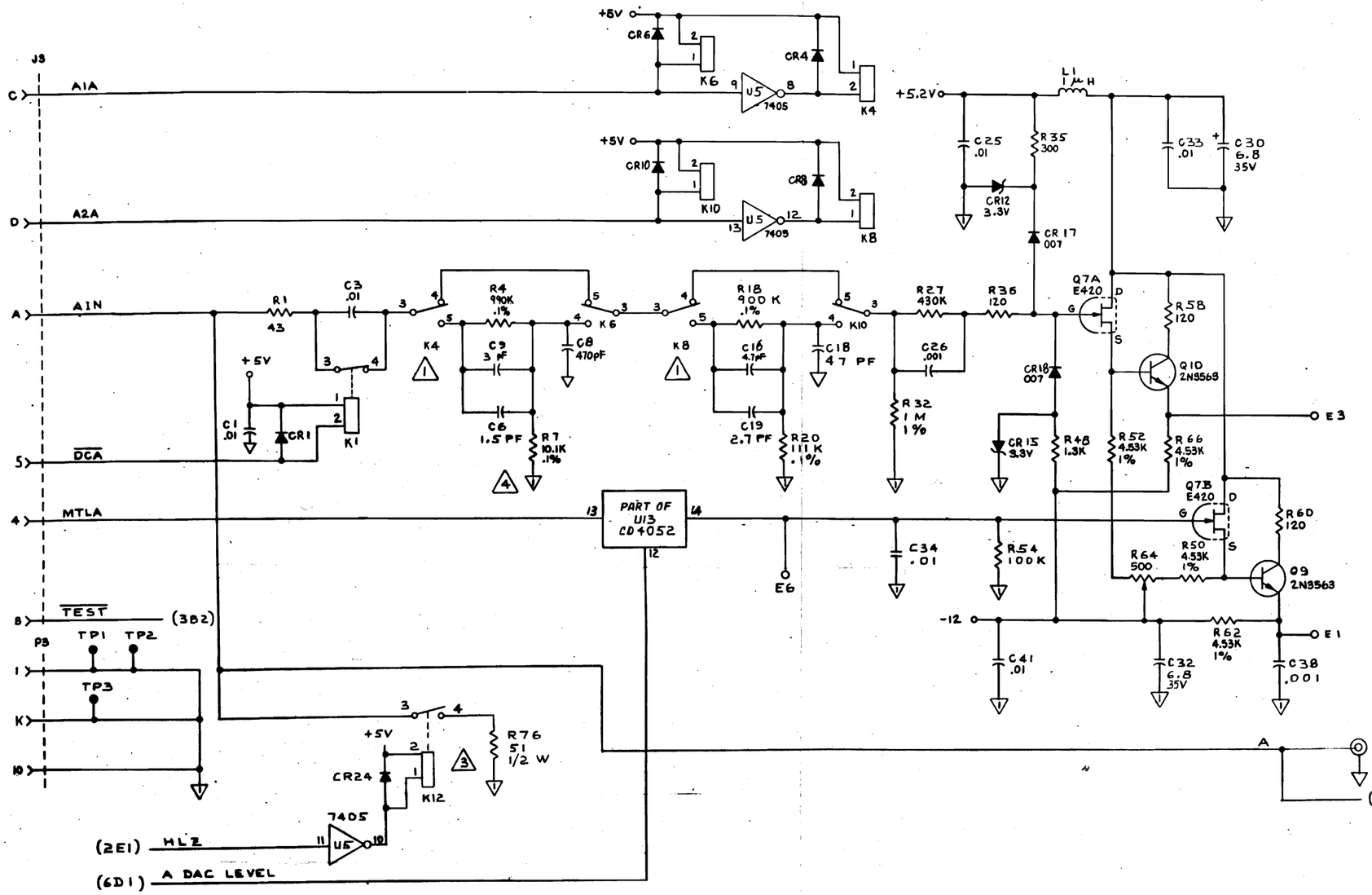
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC
IEEE-488/1975
INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721868	A

SCALE — SHEET 4 OF 6

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHT 1			



4. THE SYMBOL ▽ DENOTES SIGNAL CONDITIONER AND DAC GROUND.
3. R76, K12 AND CR24 INSTALLED WITH OPTION 55E.
2. J16 INSTALLED WITH OPTION 01.
1. RELAYS SHOWN IN ENERGIZED STATE

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406868	9514		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN		
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
IEEE - 488 / 1975
INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721868	A

SCALE — SHEET 5 OF 6

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHT 1			

TRIGGER LEVEL A REGISTER

9-BIT DAC

DAC REFERENCE GENERATOR

I-V CONVERTERS

TRIGGER LEVEL B REGISTER

9-BIT DAC

(2E1) DO A DATA

(1C1) S8 A CLOCK

(5B7) A DAC LEVEL

(4A8) B DAC LEVEL

B DATA

B CLOCK

U8 74LS74

U9 74LS164

U10 1408LS

U4 74LS164

U3 1408LS

U7 LM324

Q1 Q2 Q3 Q4 Q5 Q6 2N4248

200200

CA 3086

PART OF U11

W1 W2

⚠ THE SYMBOL ▽ DENOTES SIGNAL CONDITIONER AND DAC GROUND

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406868	9514		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	
CHECK	
DESIGN	
MECH ENGR	
PROJ ENGR	
PROD ENGR	

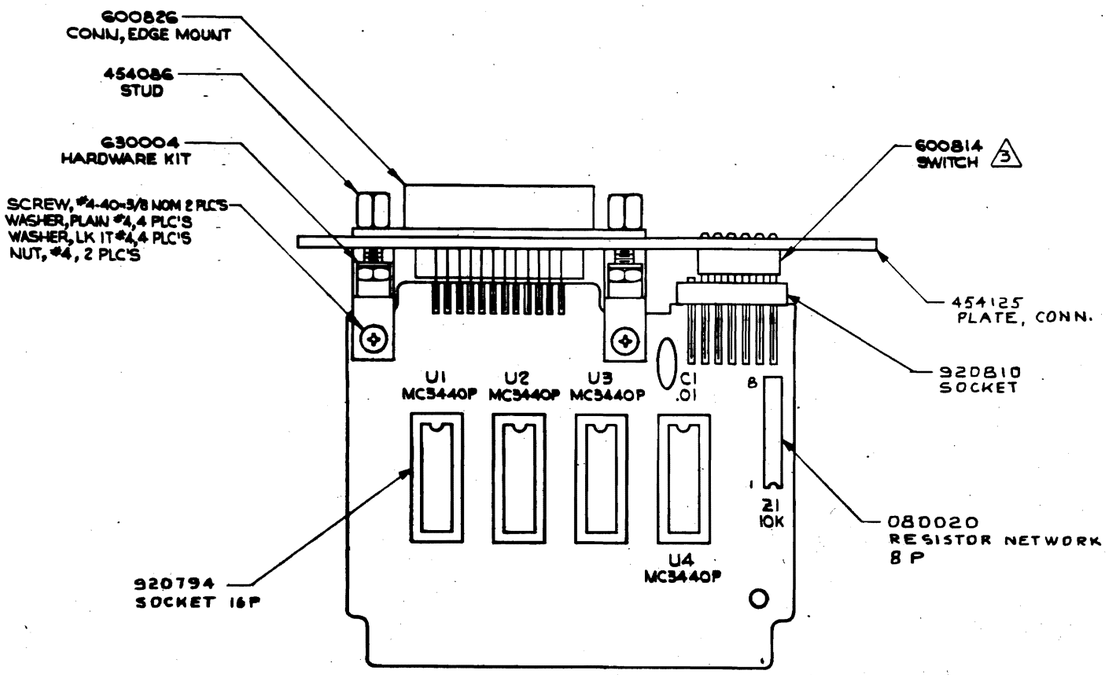
DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC
IEEE - 488/1975
INTERFACE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721868	A

SCALE — SHEET 6 OF 6

PCB REV	REVISIONS				
	LTR	DESCRIPTION		DR	CHK	APPD
A	A	RELEASED PER DRN #1149	11/7/77	[illegible]		



COMPONENT SIDE SHOWN

3 INSTALL WITH "ON" POSITION TOWARDS COMPONENT SIDE (TOP) OF PCB

2. REFERENCE SCHEMATIC NO. 721867

1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406889	9514		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN	DIGANGI	10-13-77
CHECK	[signature]	11-7-77
DESIGN		
MECH ENGR	[signature]	11-4-77
PROJ ENGR	K. McClellan	11/4/77
PROD ENGR	[signature]	11-7-77

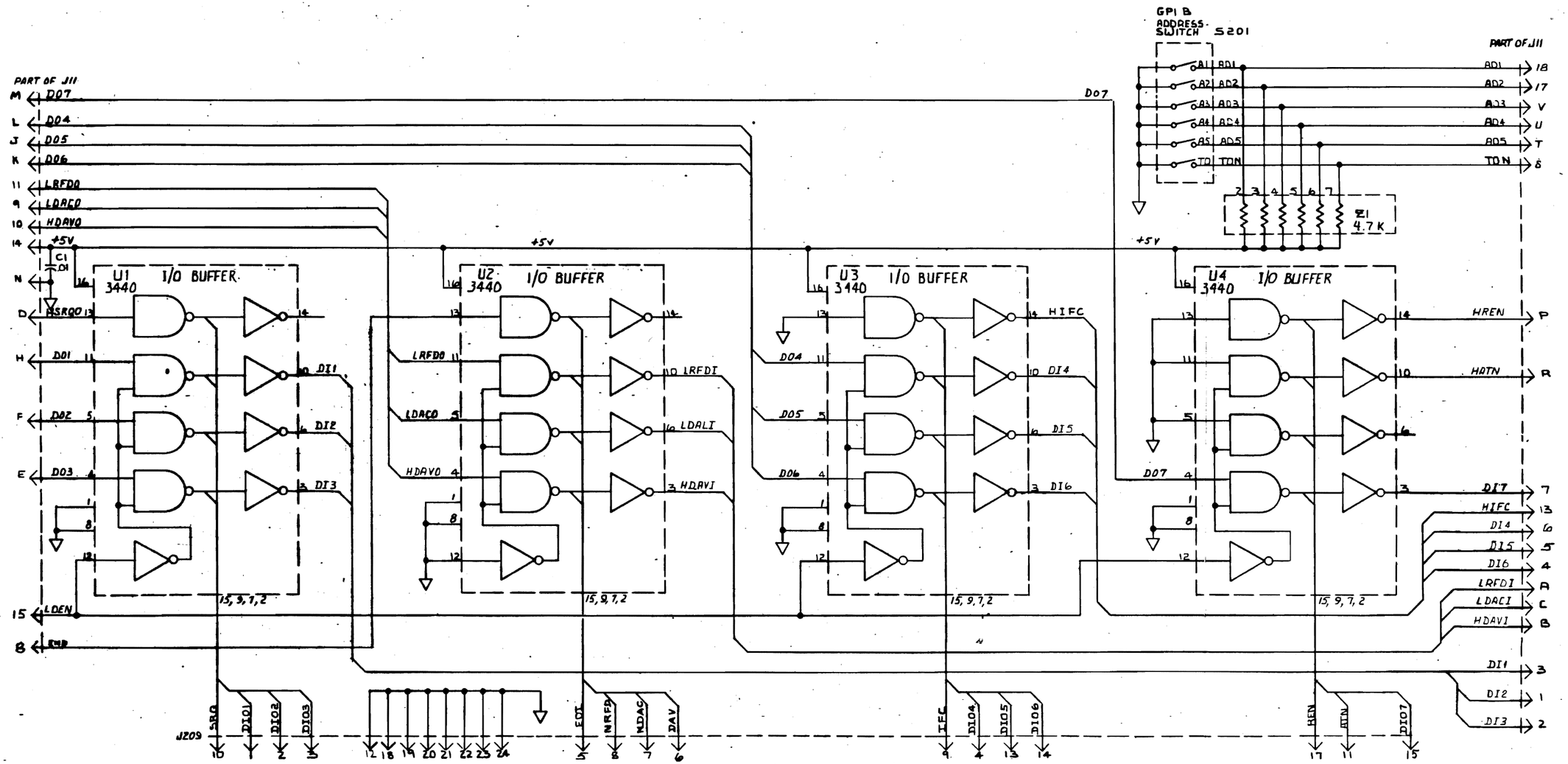
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASS'Y
I/O BUFFER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406867	A

SCALE 2/1 SHEET 1 OF 2

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
B	A	RELEASED PER DRN #			



NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406867	9514		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	H. Stickyard	4/26-78
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

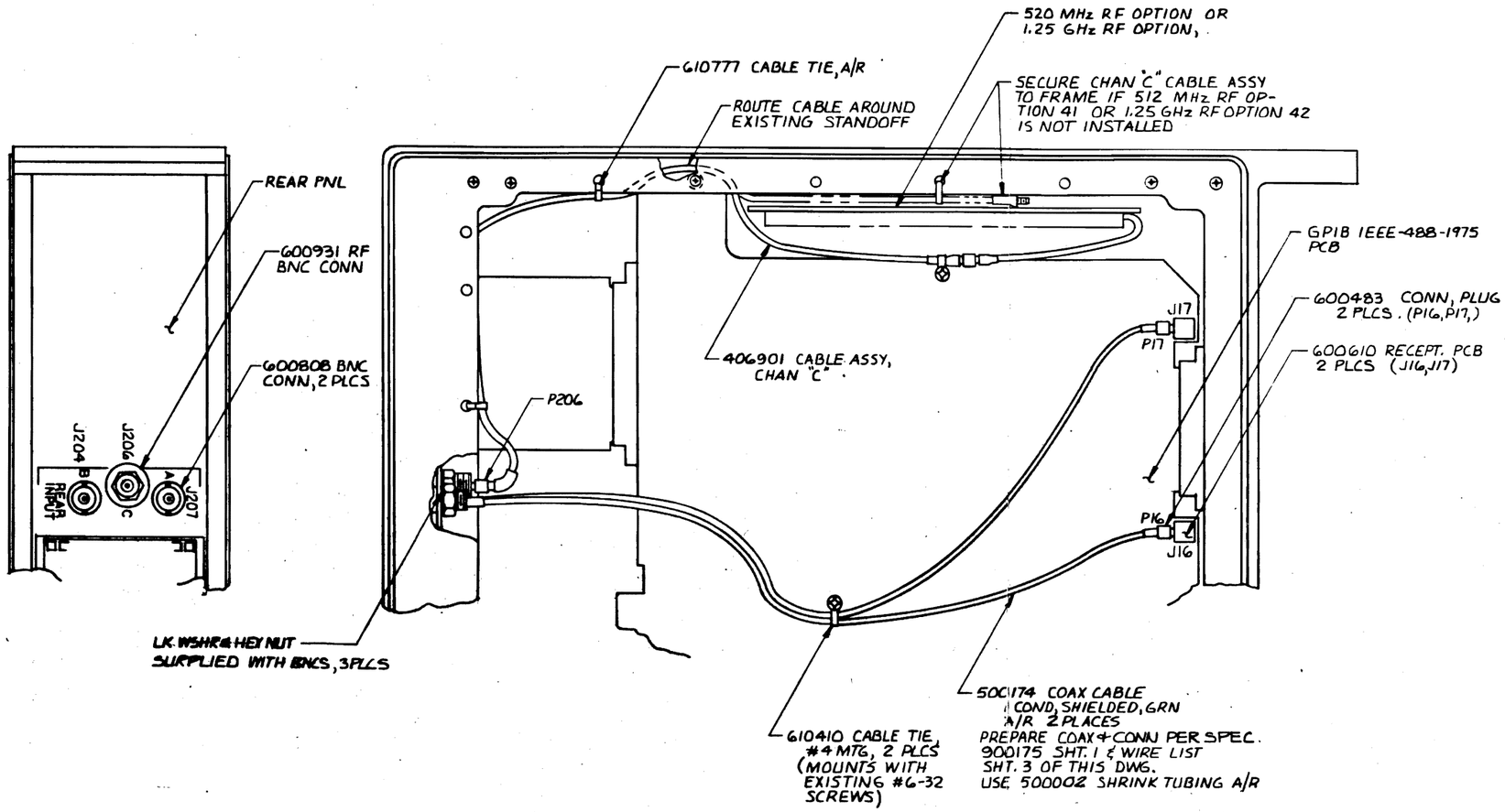
DANA LABORATORIES INC., IRVINE, CALIFORNIA

SCHEMATIC
I/O BUFFER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721867	A

SCALE ——— SHEET / OF /

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1166 4/6/78	mk	[illegible]	M



2. TYPE OPTION NO 01 ON SERIAL NO TAG USED ON BASIC ASSY UNIT
1. ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
—	9514	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Guzman	5/3/78
CHECK	[illegible]	5-30-78
DESIGN	Guzman	5/3/78
MECH ENGR	[illegible]	6-2-78
PROJ ENGR	K. McCLELLAN	6-2-78
PROD ENGR	[illegible]	6-5-78

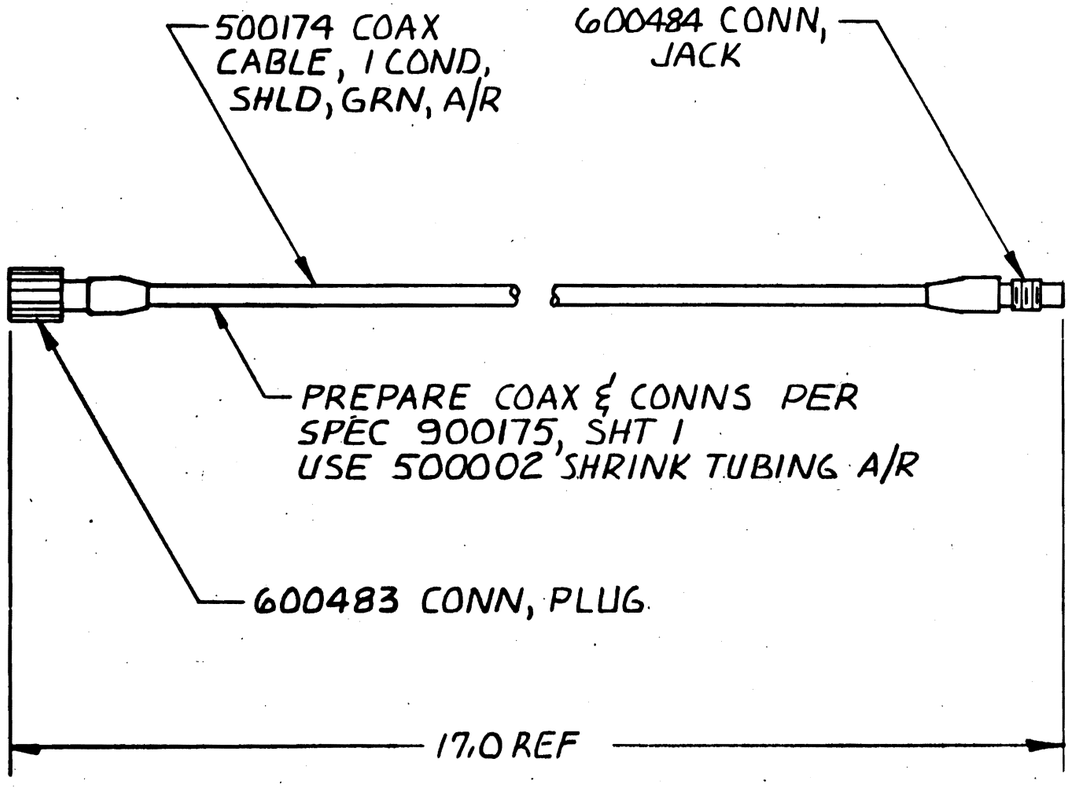
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

OPTION 01 ASSY
REAR INPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406900	A

SCALE NONE SHEET 1 OF 3

REVISIONS				
LTR	DECRIPTION	DRN	CHK	APPD
A	RELEASED PER DRN # 1166 6/6/78	MA	mayer	



2. TAG & IDENTIFY WITH RACAL-DANA P/N & CURRENT REV LTR.
1. ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

406900	9514	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Ousmon	5/4/78
CHECK	[illegible]	5-5-78
DESIGN	Ousmon	5/4/78
MECH ENGR	Guercio	6-2-78
PROJ ENGR	K. McCLELLAN	6-2-78
PROD ENGR	[illegible]	6-5-78

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

CABLE ASSY, CHAN "C"

SIZE	CODE IDENT NO.	DWG NO.	REV
B	21793	406901	A

SCALE NONE | SHEET 1 OF 2

DIETZGEN 980340 DIETZGEN-POST CLEARPRINT 1020

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PAGE
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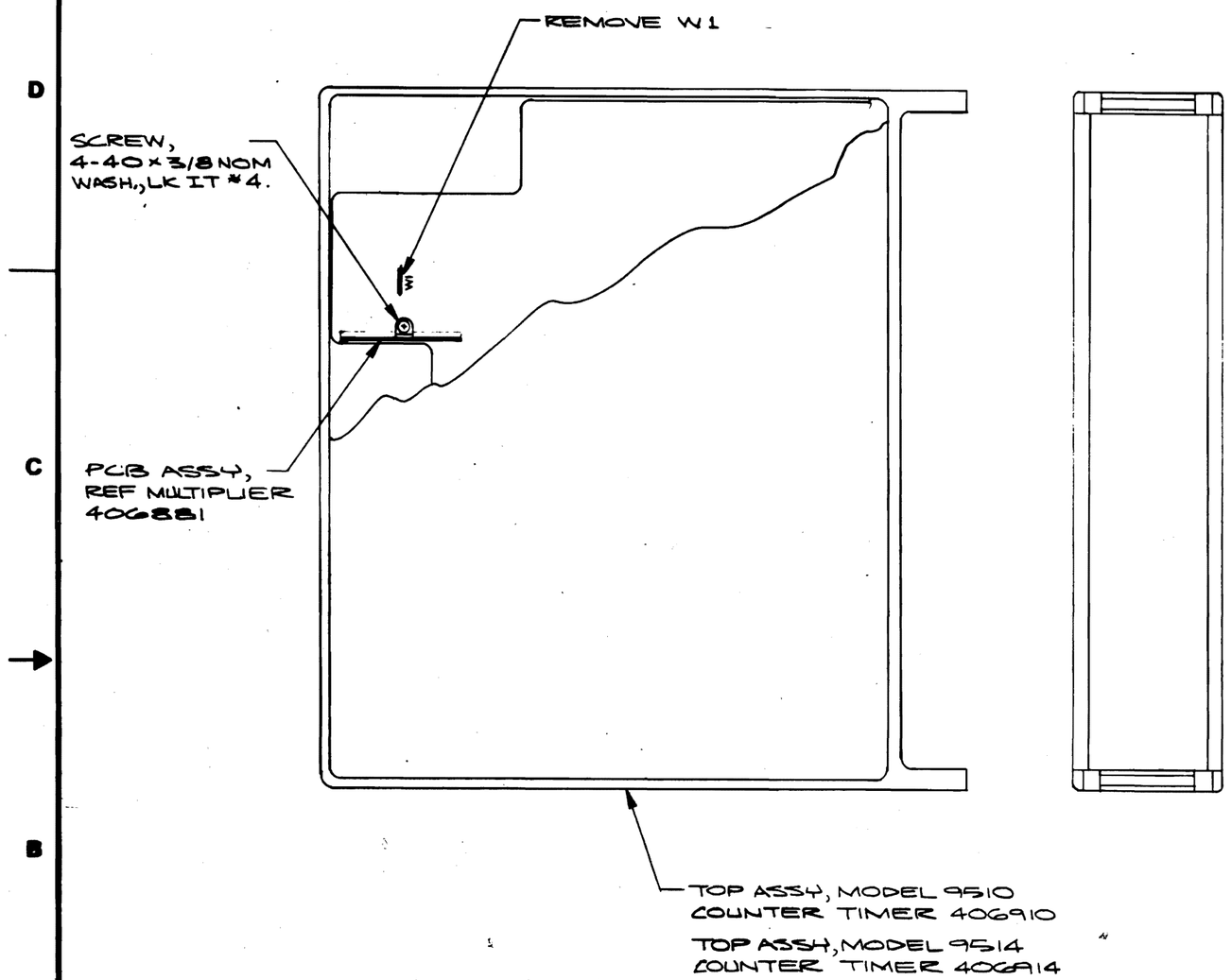
SCANS
By
Artek Media

PCB REV	REVISIONS					
	LTR	DESCRIPTION		DR	CHK	APPD
	A	RELEASED PER DRN # 1150	11/16/77	Wayne		M



1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STD'S.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	9514		1
	9510		1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	P. VENNE	11/7-77
CHECK		11/9/77
DESIGN		
MECH ENGR		11-9-77
PROJ ENGR	K. McClellan	11/9/77
PROD ENGR		11-16-77

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

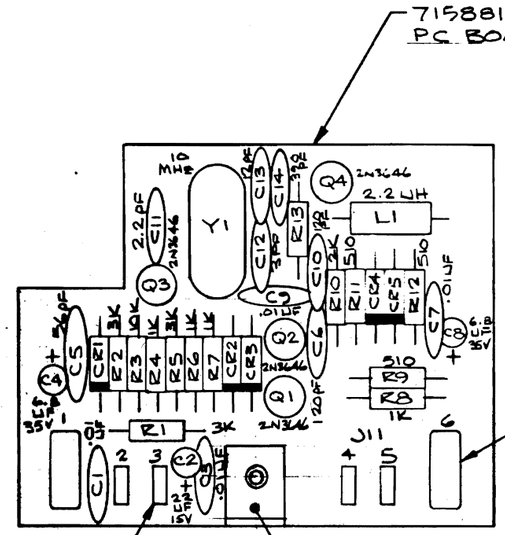
ASSY, REF MULTIPLIER

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406898	A

SCALE NONE | SHEET 1 OF 2

DANA 990337

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1149 11/7/77	mayer		
B	B	REVISED PER EO #	HS 2-22-78		



715881
P.C. BOARD

600149
RECEPTACLE
2 REQ'D

600787
RECEPTACLE
4 REQ'D

453402
BRACKET, RT. ANGLE
610427
RIVET, TUB .06 X 3/16 LG.

4. ALL DIODES ARE IN916B
3. RESISTOR VALUES ARE IN OHMS ±5%, 1/4 W.
2. REF SCHEMATIC NO 721881
1. ASSY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STD'S.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406891	9514	1	1
406890	9510	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH
/	/

DRAWN	D. MacARTHUR	OCT. 17 '77
CHECK	[signature]	11/1/77
DESIGN		
MECH ENGR	GUERCIO	11-1-77
PROJ ENGR	K. McClellan	11-1-77
PROD ENGR	[signature]	11-7-77

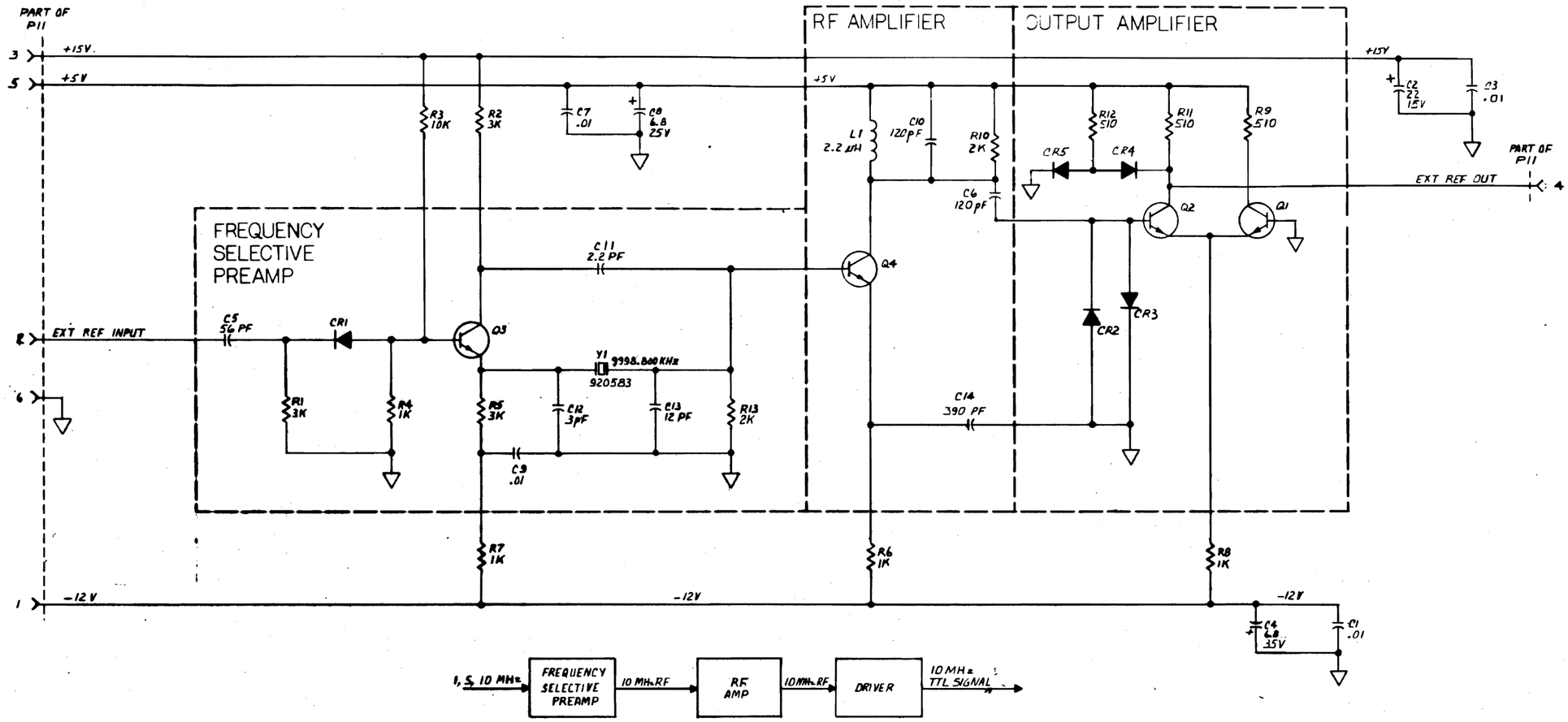
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY
REFERENCE MULTIPLIER

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406881	B

SCALE | SHEET 1 OF 3

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN #			



4. TRANSISTORS ARE 2N3646
3. DIODES ARE IN916B
2. CAPACITOR VALUES ARE IN µF
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406881	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN	H. Stickley	6/26/78
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

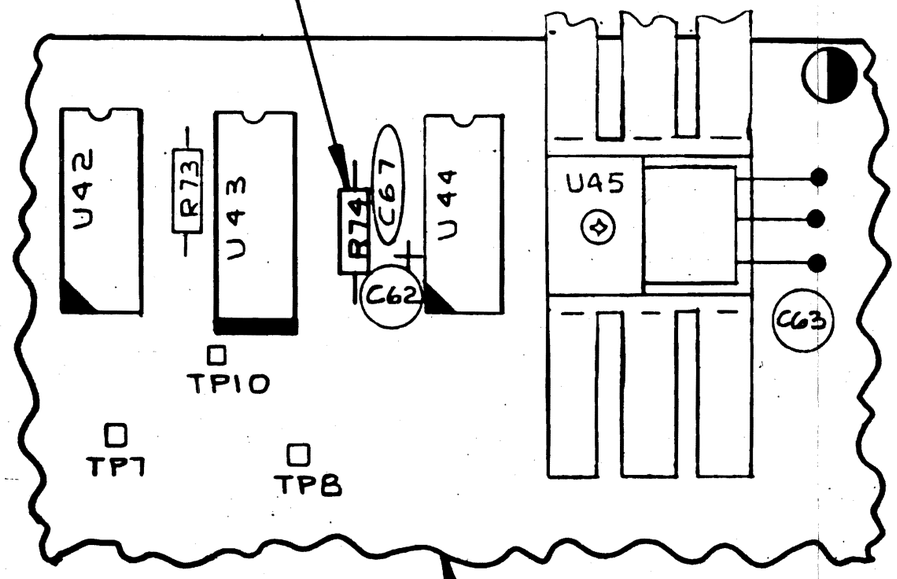
SCHEMATIC - 9500-OPT, 01
REFERENCE MULTIPLIER PCB

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721881	A

SCALE — SHEET 1 OF 1

REVISIONS				
LTR	DECRIPTION	DRN	CHK	APPD
A	RELEASED PER DRN # 1167 4/26/78	mk	mayer	

R74: REMOVE 000103 AND SCRAP,
INSTALL 000104 IN ITS PLACE



IEEE-48-1975
INTERFACE PCB ASSY.
406868 REF.

2. TYPE OPTION 12 ON SERIAL TAG USED ON BASIC ASSY UNIT.
1. ASSEMBLE PER RACAL-DANA WORK-MANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

—	9500	—	—
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Z. Bemasn	6/16/78
CHECK		6/16/78
DESIGN		
MECH ENGR	Guercio	6-16-78
PROJ ENGR	K.MCCLELLAN	6/16/78
PROD ENGR		6/16/78

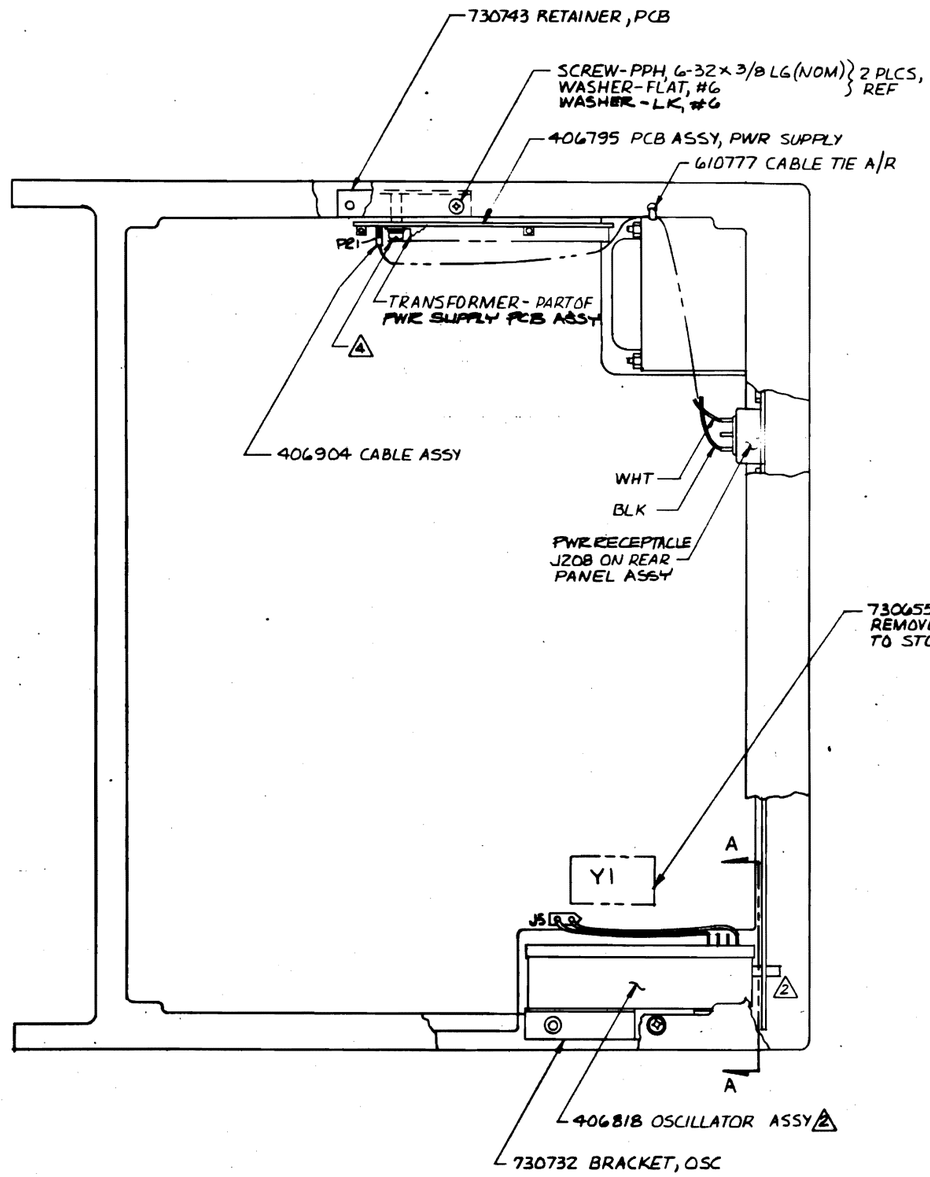
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

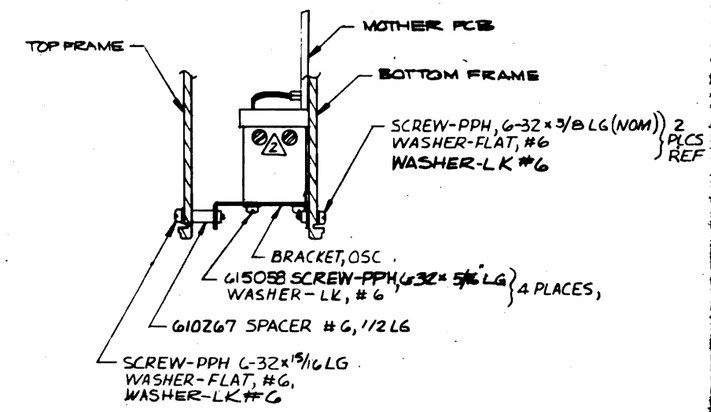
40 Hz AUTO TRIGGER ASSY. OPTION 12

SIZE	CODE IDENT NO.	DWG NO.	REV
B	21793	406912	A

SCALE NONE | SHEET 1 OF 2

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN #1166 6/6/78			





SECTION A-A
NO SCALE

4 PLUG PWR SUPPLY PCB INTO MOTHER PCB, REMOVE EXISTING HEX NUT FROM TRANSFORMER, ATTACH TO RETAINER + TOP FRAME AS SHOWN

3 TYPE OPTION NO 22 ON SERIAL NO. TAG USED ON BASIC ASSY UNIT.

2 REMOVE ADJUSTMENT PLUGS FROM OSCILLATOR PRIOR TO INSTALLATION AND REPLACE PLUGS AFTER INSTALLATION.

1. ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL.

NOTE: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	2514		
	2510		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN		5/31/78
CHECK		5-30-78
DESIGN		5/31/78
MECH ENGR		6-2-78
PROJ ENGR	K. MCCLELLAN	6-2-78
PROD ENGR		

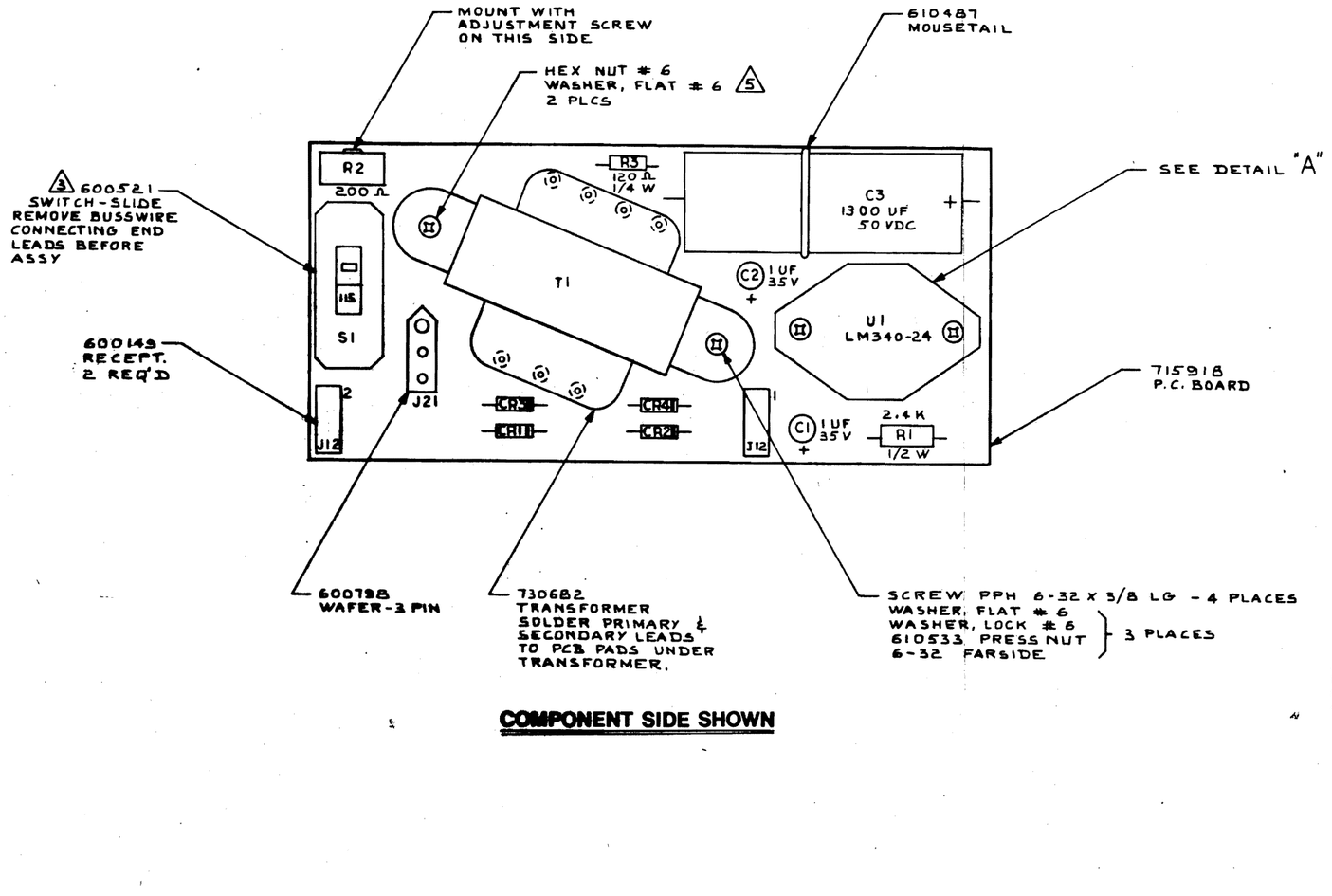
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

OPTION #22 ASSY,
OVEN OSCILLATOR $<1 \times 10^{-9}$

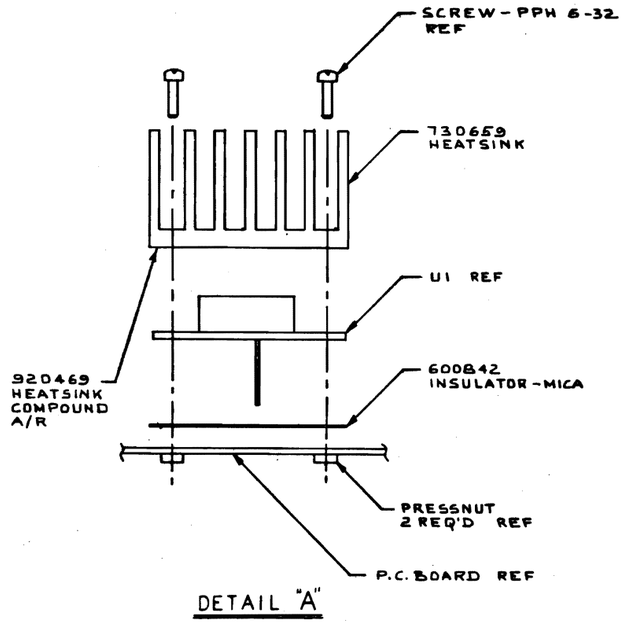
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406902	A

SCALE NONE SHEET 1 OF 2

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1167			



COMPONENT SIDE SHOWN



DETAIL "A"

△5 TO INSURE AGAINST PCB WARPAGE INSTALL #6 FLAT WASHER BETWEEN TRANSFORMER BRKT & PCB

4. ALL DIODES ARE 210004

△3 SWITCH S1 S/B RAISED OFF PCB ± .125

2. REFERENCE SCHEMATIC NO. 721918

1. ASSEMBLY PROCESS AND PROCEEDURES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

406903	9500 OPT. 24	1	1
406902	9500 OPT. 22	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN		6-14-78
CHECK		6-18-78
DESIGN		6-19-78
MECH ENGR		6-22-78
PROJ ENGR		7-1-78
PROD ENGR		6-22-78

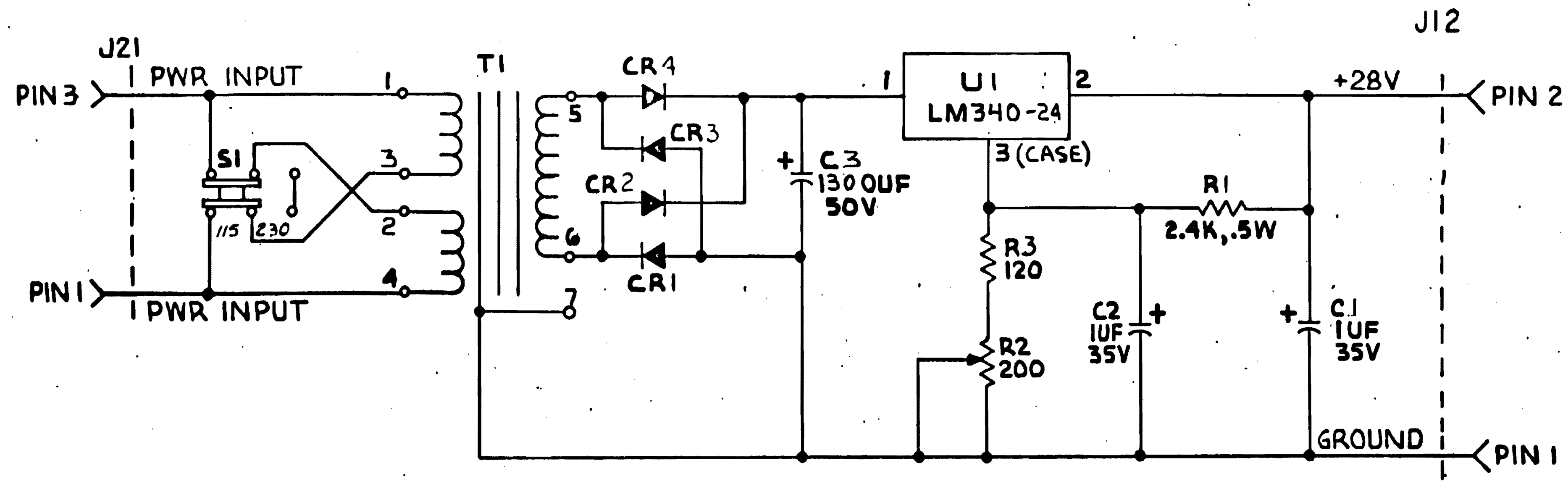
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSY POWER SUPPLY OVEN OSCILLATOR

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406918	A

SCALE 2/1 SHEET 1 OF 3

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1167 6/30/78			



NOTES: UNLESS OTHERWISE SPECIFIED
1. DIODES ARE SD4.

406918	9500	REF	REF
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN MILLIMETERS AND INCLUDE THICKNESS OF PLATING

TOLERANCES: DECIMALS .X ± .5, .XX ± .25; ANGLES ± 0° 30′, FORMED ± 1° 0′; HOLE DIAMETERS +.10 −.05

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	H. Shidleyd	6-14-78
CHECK		6/24/78
DESIGN	H. Shidleyd	6-14/78
MECH ENGR	Guerecio	6-28-78
PROJ ENGR	K McClellan	6/2
MFG ENGR		

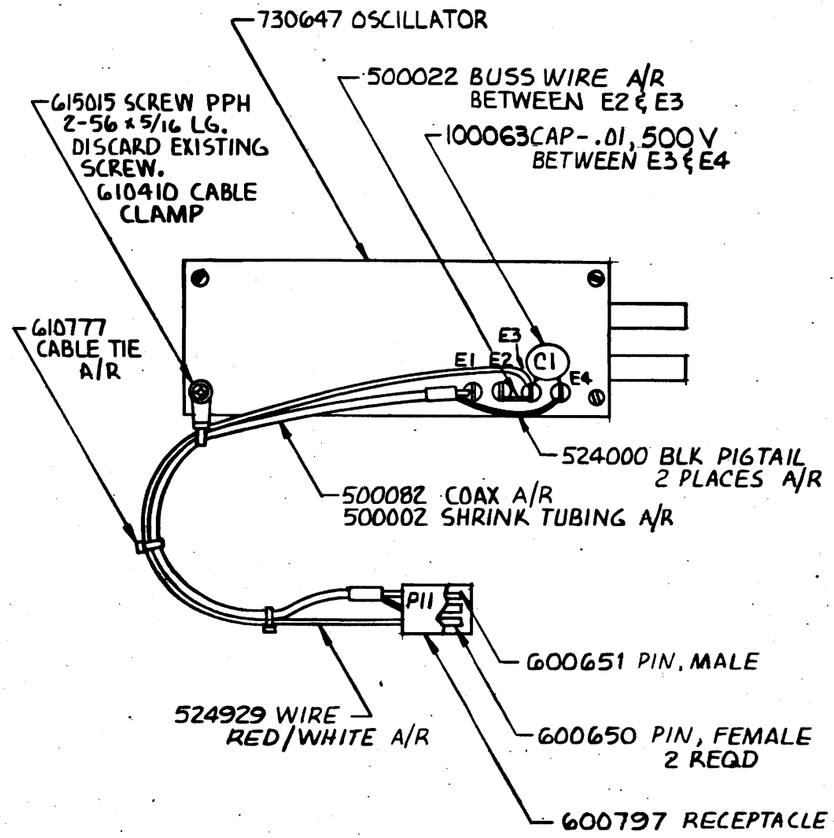
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
POWER SUPPLY
OVEN OSCILLATOR

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	721918	A

SCALE — SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1111	1/23/75	75	
B	REVISED PER E.O. 10729	J.D. 12-6-77	1-11-78	



WIRE LENGTHS

COAX CABLE ——— 6.5 ±.25
RED/WHITE WIRE — 7.0 ±.25

1. ASSEMBLY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

406805	9000 OPT.22	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Auoman	12/18/75
CHECK	G. Mooney	12/19/75
DESIGN	Auoman	12/18/75
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

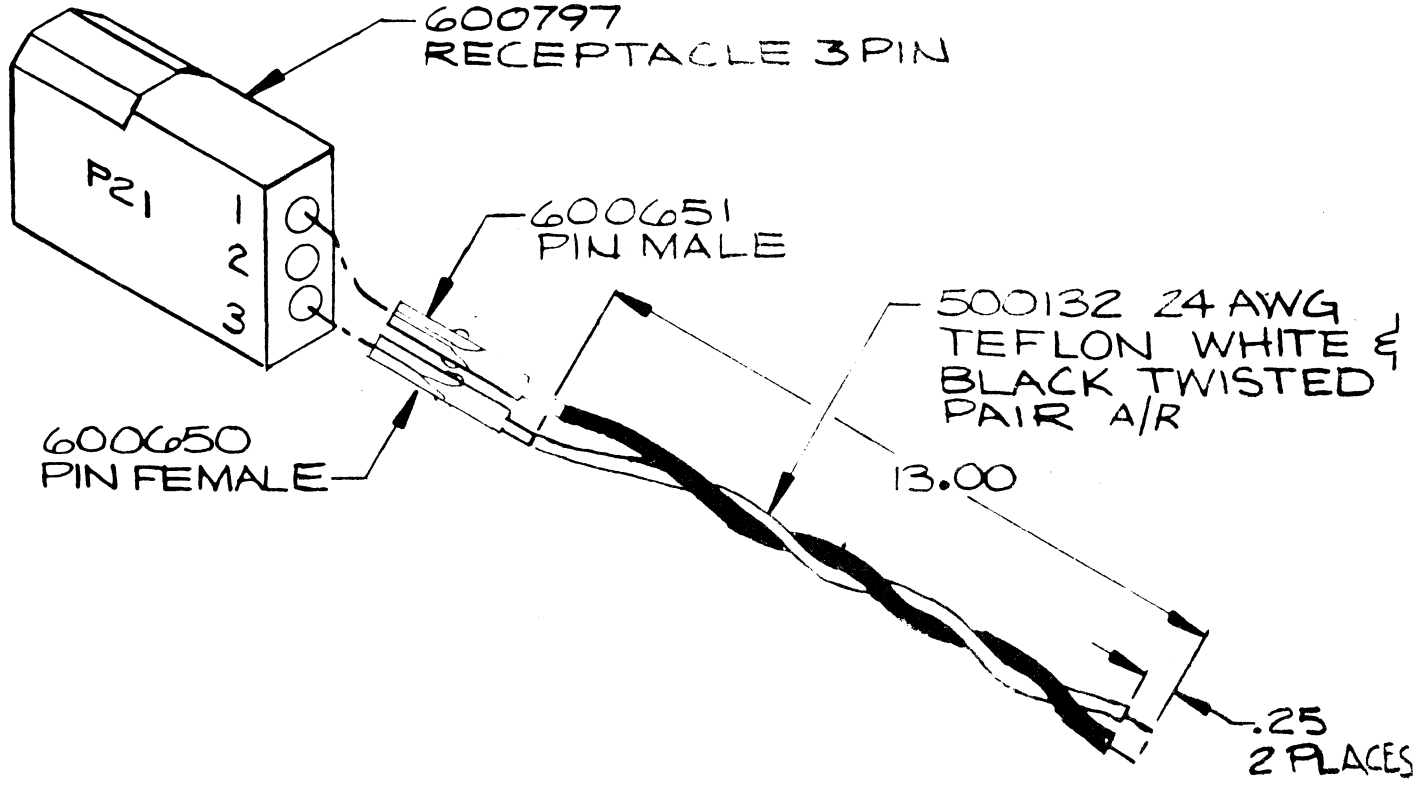
ASSY-OSCILLATOR, OPT.22

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406818	B

SCALE NONE | SHEET 1 OF 2

APPLICATION	
NEXT DWG	USED ON
406902	9510-9514
406903	9510-9514

REVISIONS					
LTR	DESCRIPTION		DRN	CHK	APPD
A	RELEASED PER DRN # 1166	6/6/78	MK	[illegible]	



2 TAG AND IDENTIFY WITH RACAL-DANA P/N CURRENT REV LTR

1 ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	—.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.5

MATERIAL / FINISH

DRAWN	BKING	5-5-78
CHECK	[illegible]	5-25-78
DESIGN	Ausmon	4/5/78
MECH ENGR	G UEBELACKER	6-2-78
PROJ ENGR	K MCCLELLAN	6-2-78
PROD ENGR	[illegible]	6-5-78

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

CABLE ASSY. AC POWER

SIZE	CODE IDENT NO.	DWG NO.	REV
A	21793	406904	A

SCALE NONE | SHEET 1 OF 2

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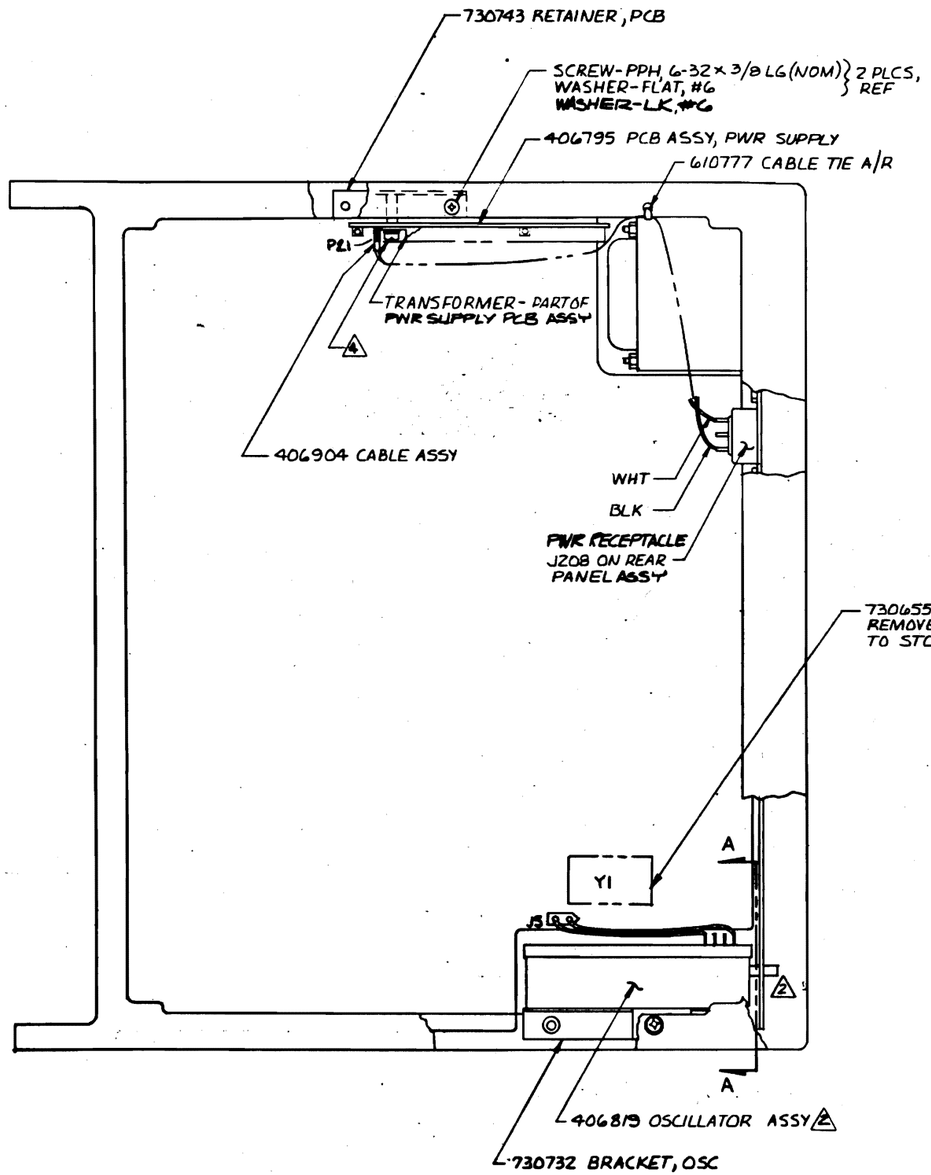
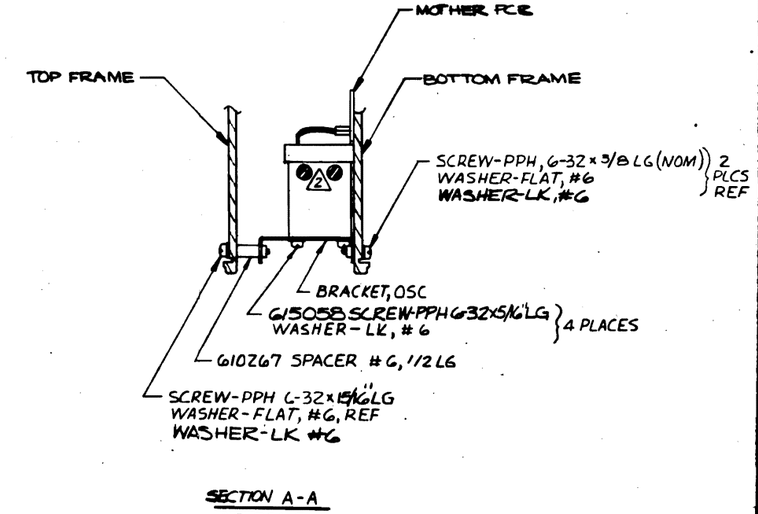
PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1166 6/6/78	JH	mayo	M





SECTION A-A
NO SCALE

4 PLUG PWR SUPPLY PCB INTO MOTHER PCB, REMOVE EXISTING HEX NUT FROM TRANSFORMER, ATTACH TO RETAINER + TOP FRAME AS SHOWN

3 TYPE OPTION NO 24 ON SERIAL NO TAG USED ON BASIC ASSY UNIT.

2 REMOVE ADJUSTMENT PLUGS FROM OSCILLATOR PRIOR TO INSTALLATION AND REPLACE PLUGS AFTER INSTALLATION.

1. ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL.

NOTE: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
—	9514	—	—
—	9510	—	—
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	J. Harmon	4/5/78
CHECK	[illegible]	5-31-78
DESIGN	J. Harmon	4/5/78
MECH ENGR	G. Garcia	6-2-78
PROJ ENGR	K. McClellan	6-2-78
PROD ENGR	[illegible]	6-5-78

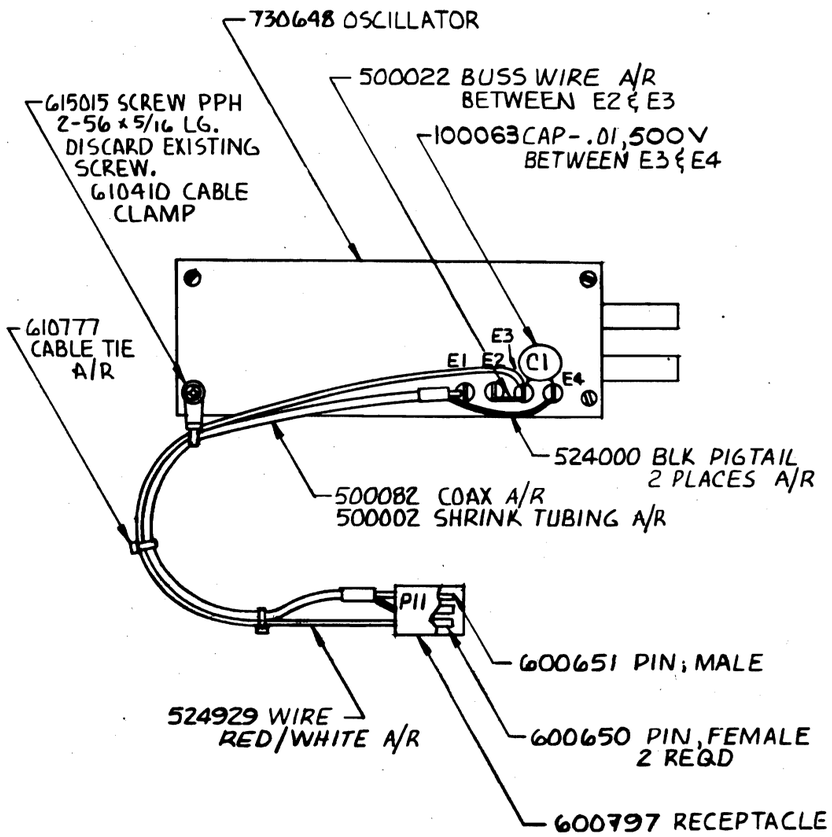
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

OPTION 24 ASSY
OVEN OSCILLATOR $<5\times10^{-10}$

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406903	A

SCALE NONE SHEET 1 OF 2

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1111	12/23/75		
B	REVISED PER E.O. 10730	J.D. 12-6-77	1-11-78	



WIRE LENGTHS

COAX CABLE ——— 6.5 ±.25
RED/WHITE WIRE – 7.0 ±.25

1. ASSEMBLY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

406806	9000 OPT. 24	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Aronson	12/18/75
CHECK	G. Whorway	12/18/75
DESIGN	Aronson	12/18/75
MECH ENGR		
PROJ ENGR	G. Whorway	12/24/75
PROD ENGR		

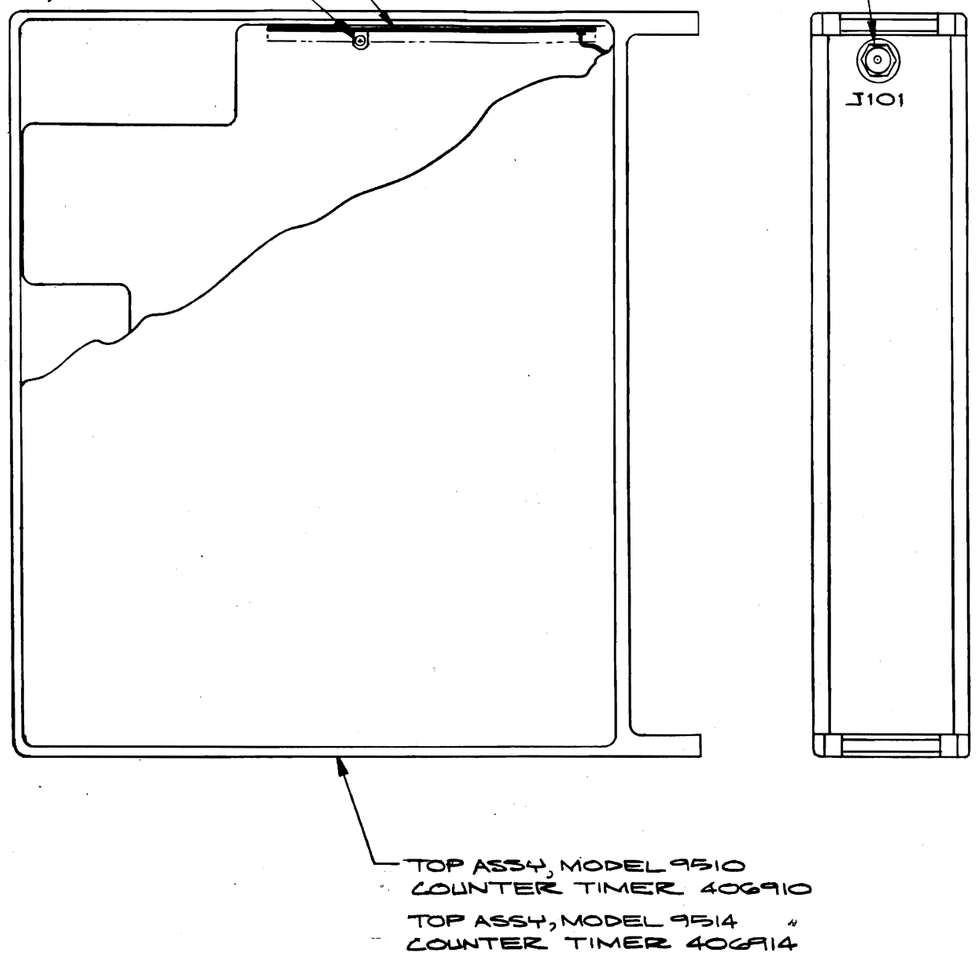
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY-OSCILLATOR, OPT. 24

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406819	B

SCALE NONE | SHEET 1 OF 2

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1150 11/16/77	wayne		



1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STD'S.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
——	9514		1
——	9510		1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	B. VENNE	11/7/77
CHECK		11/7/77
DESIGN		
MECH ENGR		11.9.77
PROJ ENGR	K. McClellan	11/9/77
PROD ENGR		11/16/77

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

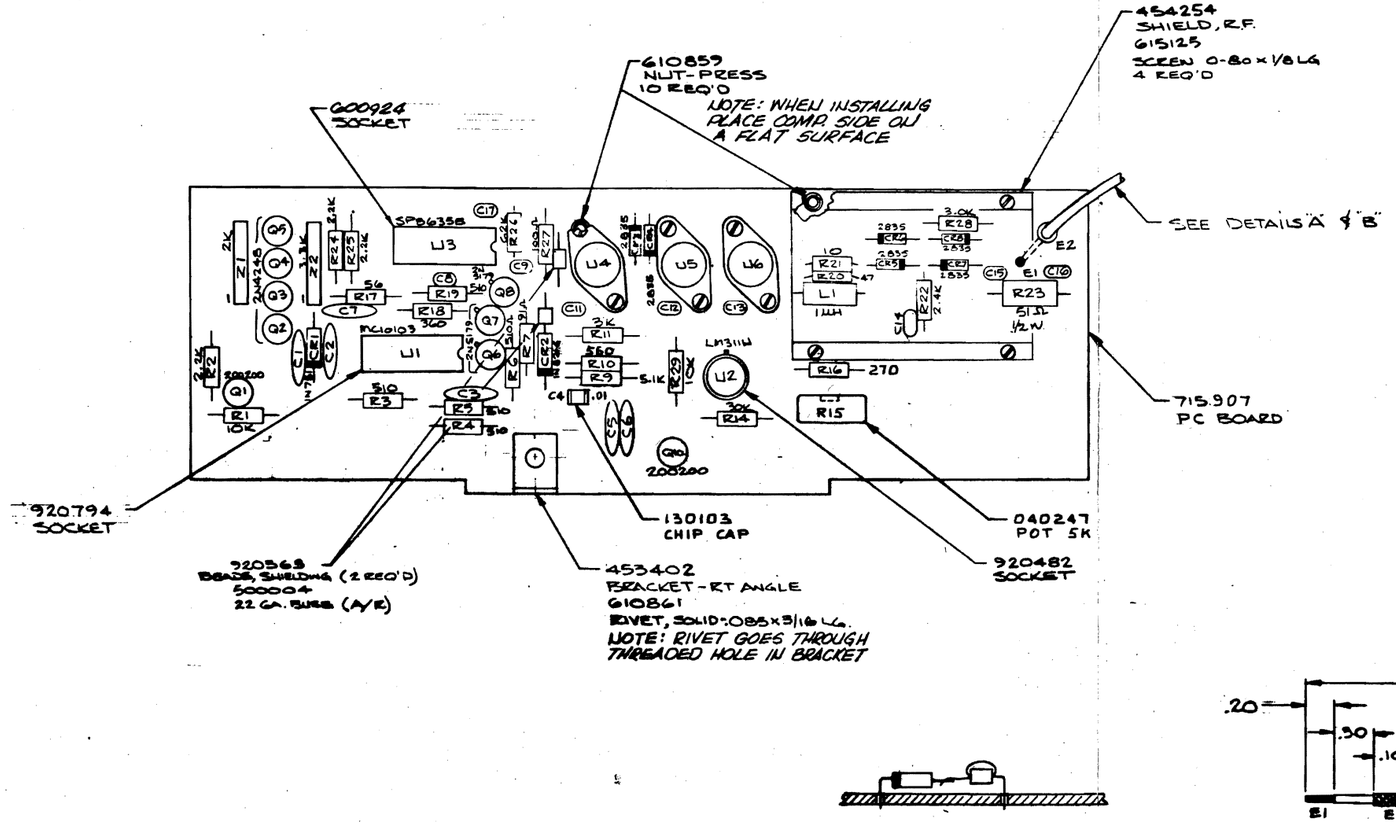
ASSY, 512 MHz RF

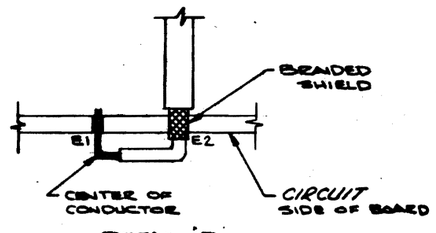
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406897	A

SCALE NONE | SHEET 1 OF 2

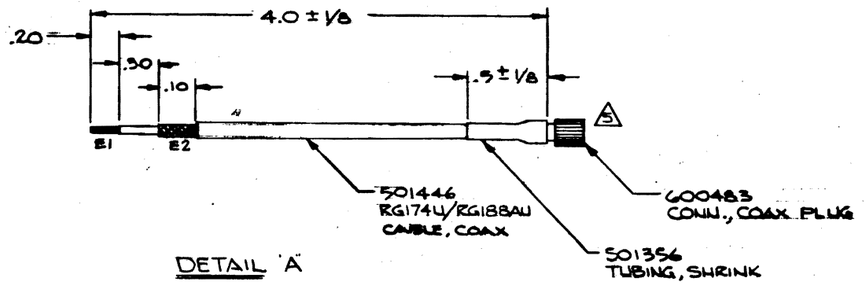
DANA 980337

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1163 4/5/78	mayes		M
A	B	REVISED PER EO# 11784	H.S. 6-27-78		
A	C	REVISED PER EO #	H.S. 6-29-78		





DETAIL 'B'



DETAIL 'A'

⚠2 CENTER CONDUCTOR OF CABLE TO BE TERMINATED TO CENTER PIN OF CONNECTOR

4. CAPACITOR VALUES ARE .01 MF, 100V
3. RESISTOR VALUES ARE IN OHMS ±5% 1/4W
2. REF SCHEMATIC NO. 721907
1. ASSY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

406897	9500		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	M. Anderson	3/21/78
CHECK		3/21/78
DESIGN		
MECH ENGR		3-21-78
PROJ ENGR	K. McGee	3/24/78
PROD ENGR		3-24-78

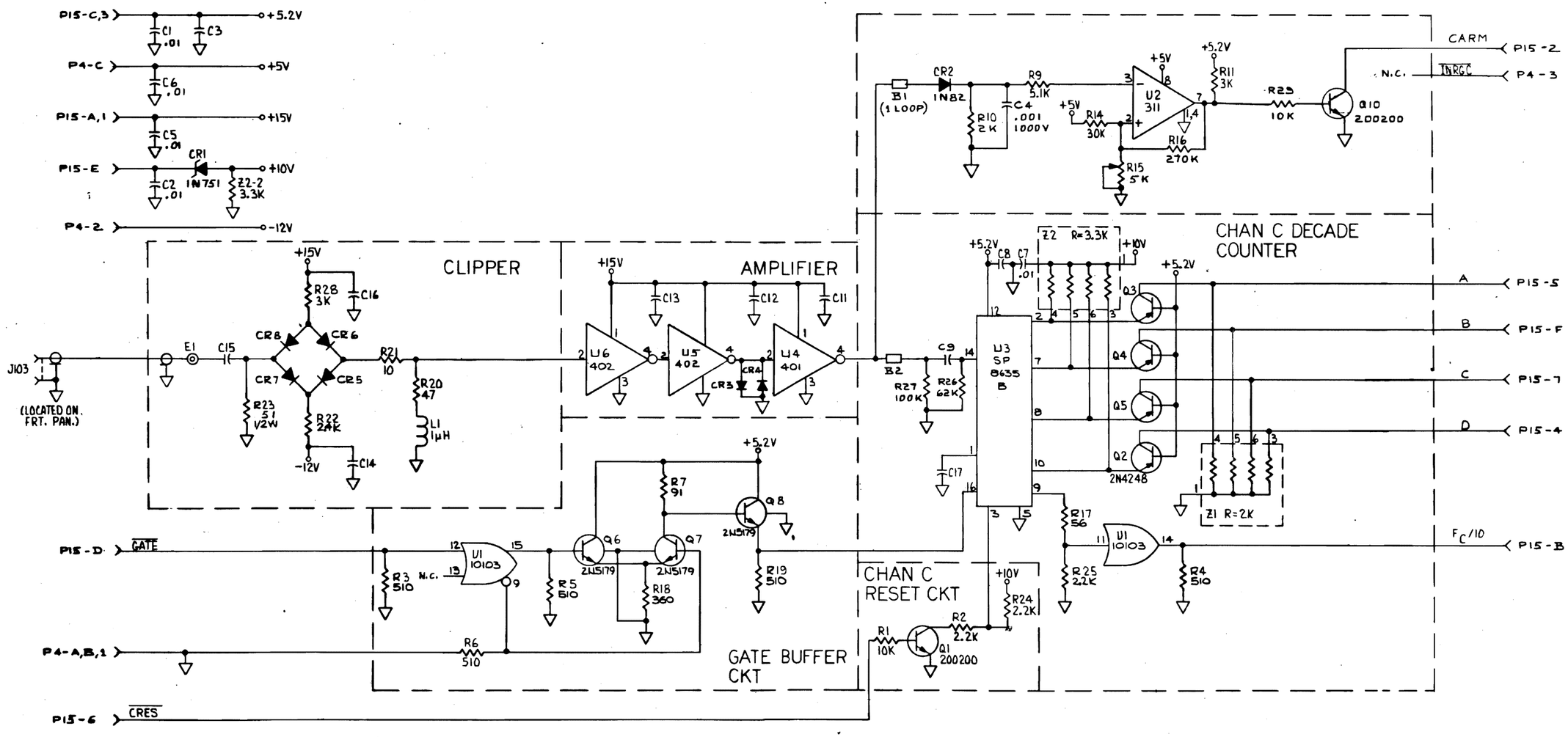
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY
R.F. 512 MHz

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406907	C

SCALE 2/1 SHEET 1 OF 5

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN #			



4, C8, C9, C11 THRU C17 ARE .01uF, 100V, 10%
3. DIODES ARE HP 5082-2835
2. CAPACITORS ARE .01uF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
406907	9500		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Rich Mays	12-15-77
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

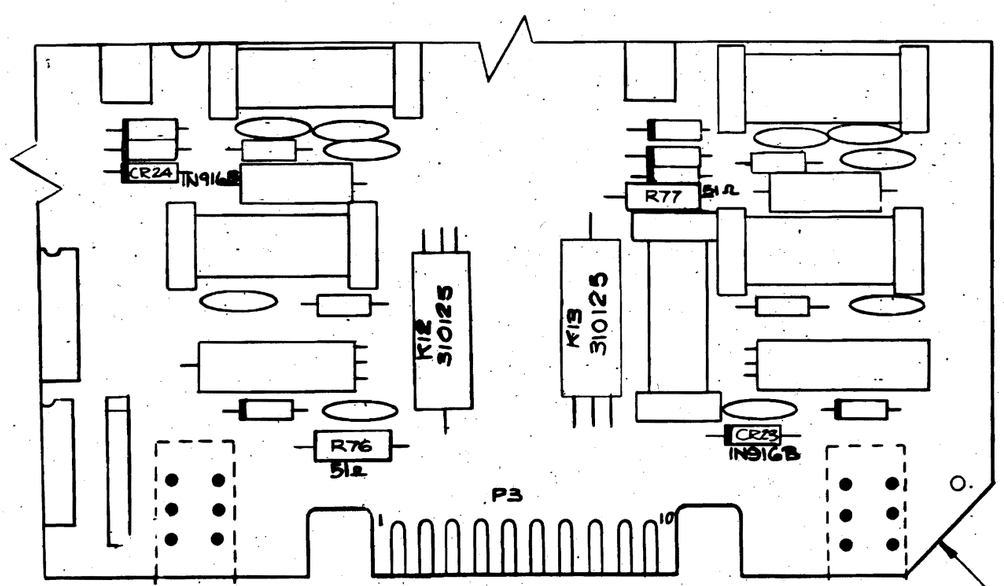
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

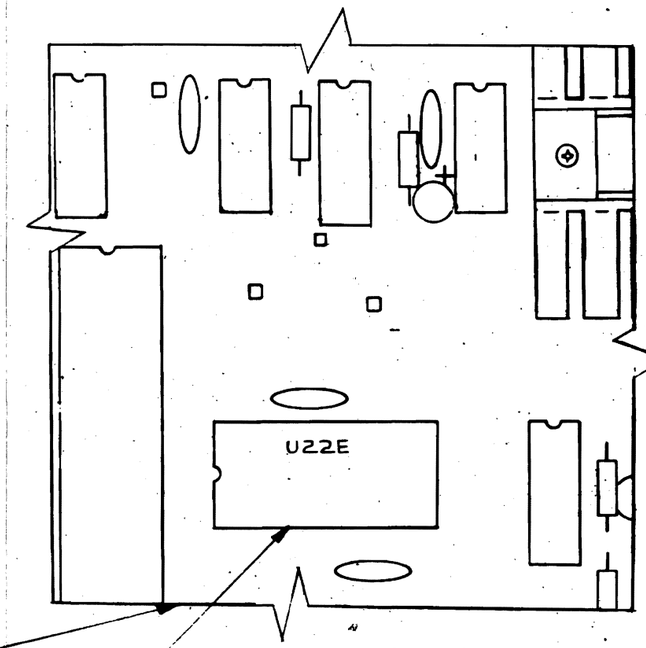
SCHEMATIC - 9500 512 MHz RF PCB

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721907	A

SCALE | SHEET 1 OF 1

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1166 6/6/78	MR	[illegible]	[illegible]





IEEE-488-1975 INTERFACE PCB ASSY 406868 REF

REMOVE I.C. ROM U22 AND RETURN TO STOCK, AND INSTALL U22E

2 TYPE OPTION NO #55E ON SERIAL NO TAG USED ON BASIC ASSY UNIT

1 ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
—	9514	—	—
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	BKING	5-31-78
CHECK	[signature]	6/6/78
DESIGN		
MECH ENGR	Guercio	6-6-78
PROJ ENGR	K. McClellan	6-6-78
PROD ENGR	[signature]	6-6-78

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

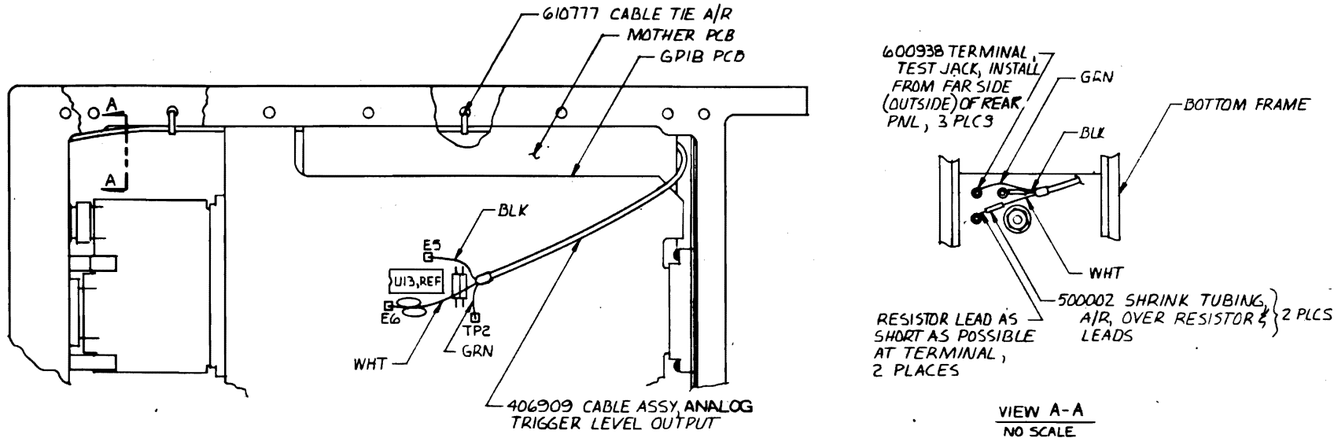
EXTENDED PROGRAMMING ASSY, OPTION #55E

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406911	A

SCALE 2/1 SHEET 1 OF 2

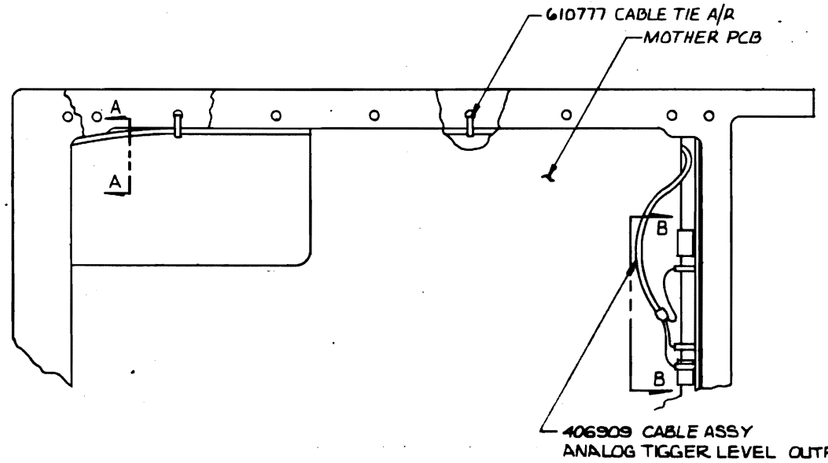
DANA 980337

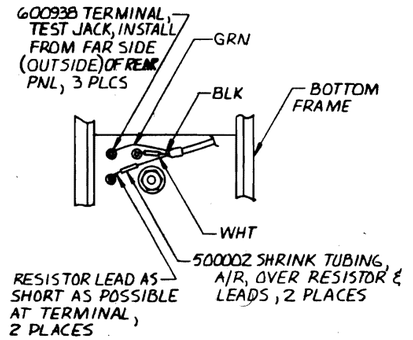
PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1166	4/6/78	MK	[illegible]



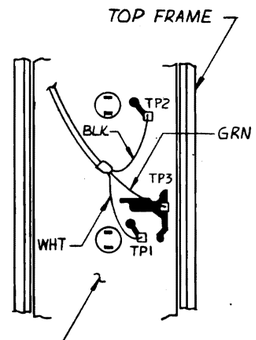
VIEW A-A
NO SCALE

ANALOG TRIGGER LEVEL OUTPUT OPTION, MODEL 9514





VIEW A-A
NO SCALE



VIEW B-B
NO SCALE

ANALOG TRIGGER LEVEL OUTPUT OPTION, MODEL 9510

2. TYPE OPTION NO 70 ON SERIAL NO TAG USED ON BASIC ASSY UNIT
1. ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
—	9510/9514	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	[illegible]	4/20/78
CHECK	[illegible]	5/1/78
DESIGN	[illegible]	4/21/78
MECH ENGR	GUERCIO	6-2-78
PROJ ENGR	K. MCCLELLAN	6-2-78
PROD ENGR	[illegible]	6-5-78

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

OPTION 70 ASSY, ANALOG TRIGGER LEVEL OUTPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406906	A

SCALE NONE | SHEET 1 OF 2

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SECTION 4 PARTS LIST

4.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

4.2 Manufacturers are identified by FSC numbers listed in table 4.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

4.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 4.1 along with the commercial equivalent.

Table 4.1

Semiconductor Type:		Equivalent:
007	Diode	Fairchild FD300

Table 4.2 - List of Suppliers

FSC	NAME	FSC	NAME
00779	AMP, INC. HARRISBURG, PA.	16733	CABLEWAVE SYSTEMS, INC. NORTH HAVEN, CONNECTICUT
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS	17856	SILICONIX, INC. SANTA CLARA, CA.
02660	AMPHENOL CORP. BROADVIEW, ILLINOIS	21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CA.
04222	AEROVOX CORP. (Hi-Q Div.) MYRTLE BEACH, SO. CAROLINA	24539	AVANTEK, INC. SANTA CLARA, CA.
04713	MOTOROLA, INC. (Semi-Conductor Products Div.) PHOENIX, ARIZONA	27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CA.
05397	UNION CARBIDE CORP. (Materials Systems Div.) CLEVELAND, OHIO	27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
07263	FAIRCHILD (Semiconductor Div.) MOUNTAIN VIEW, CA.	34371	HARRIS SEMICONDUCTOR MELBOURNE, FLORIDA
11236	CTS BERNE, INC. BERNE, INDIANA	34649	INTEL SANTA CLARA, CA.
11237	CTS KEENE, INC. PASO ROBLES, CA.	50434	HEWLETT-PACKARD CO. (HPA Div.) PALO ALTO, CA.
15636	ELEC-TROL, INC. SAUGUS, CA.	52648	PLESSEY MEMORIES SANTA ANA, CA.
		56289	SPRAGUE ELECTRIC CO. (Pacific Div.) LOS ANGELES, CA.

Table 4.2 - List of Suppliers continued

FSC	NAME
71450	CTS CORP. ELKHART, INDIANA
71471	AEROVOX CORP. (Cinema Plant) MONCKS CORNER, SO. CAROLINA
71590	CENTRALAB ELECTRONICS MILWAUKEE, WISCONSIN
71785	TRW ELECTRONIC COMPONENTS (Cinch Div.) ELK GROVE VILLAGE, ILLINOIS
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PA.
73138	BECKMAN INSTRUMENTS, INC. FULLERTON, CA.
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
76493	MILLER, J.W. CO. COMPTON, CA.
79727	C-W INDUSTRIES WARMINSTER, PA.
80031	MEPCO-ELECTRA MORRISTOWN, N.J.
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
83125	NYTRONICS, INC. DARLINGTON, SO. CAROLINA
86884	RCA (Electronics Components Div.) HARRISON, N.J.
98291	SEALECTRO CORP. MAMARONECK, N.Y.
99800	AMERICAN PRECISION INDUSTRIES, INC. (Delevan Div.) East Aurora, N.Y.

406882 – Assy., PANEL, REAR

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C201	100111	CAP	CERAM	.01 MFD	2000 V		71471	HVD6-2KV
C202	100111	CAP	CERAM	.01 MFD	2000 V		71471	HVD6-2KV
C203	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C204	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C205	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C206	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
F201	920205	FUSE	GLASS	.75 AMP	250 V		75915	3AG3%4ASB
J201	600567	CONN	RECPTLE				02660	31-236
J202	600567	CONN	RECPTLE				02660	31-236
J203	600567	CONN	RECPTLE				02660	31-236
J205	600567	CONN	RECPTLE				02660	31-236
J208	600619	CONN	RECPTLE				82389	EAC-301
T201	730725	TRANSFORMER					21793	730725
U201	230275	IC			MC7805-CT		04713	MC7805-CT
U202	230201	IC			MC7912-CP		04713	MC7912-CP
U203	230373	IC			7815-CT		04713	7815-CT
U204	230275	IC			MC7805-CT		04713	MC7805-CT

406883 – Assy., PANEL, REAR

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C201	100111	CAP	CERAM	.01 MFD	2000 V		71471	HVD6-2KV
C202	100111	CAP	CERAM	.01 MFD	2000 V		71471	HVD6-2KV
C203	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C204	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C205	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C206	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
F201	920205	FUSE	GLASS	.75 AMP	250 V		75915	3AG3%4ASB
J201	600567	CONN	RECPTLE				02660	31-236
J202	600567	CONN	RECPTLE				02660	31-236
J203	600567	CONN	RECPTLE				02660	31-236
J205	600567	CONN	RECPTLE				02660	31-236
J208	600619	CONN	RECPTLE				82389	EAC-301
T201	730725	TRANSFORMER					21793	730725
U201	230275	IC			MC7805-CT		04713	MC7805-CT
U202	230201	IC			MC7912-CP		04713	MC7912-CP
U203	230373	IC			7815CT		04713	7815CT
U204	230275	IC			MC7805-CT		04713	MC7805-CT

406869 – Assy., PCB, MOTHERBOARD

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C8	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C11	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C16	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C17	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C18	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C20	100099	CAP	CERAM	30 PFD	1000 V	5%	56289	C030B102F300J
C21	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C23	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C24	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C25	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C26	110140	CAP	TANTA	47 MFD	6 V	20%	05397	T368B476M006AS
C27	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C28	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C29	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C30	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C31	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C32	110140	CAP	TANTA	47 MFD	6 V	20%	05397	T368B476M006AS
C33	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C34	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C35	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C36	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C37	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C38	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035
C39	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C40	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C41	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M

406869 – Assy., PCB, MOTHERBOARD

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C42	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C43	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C44	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C45	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C46	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C47	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C48	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C49	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C50	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C51	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C52	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C53	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C54	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C55	110129	CAP	TANTA	.1 MFD	35 V	20%	05397	T368A104M035AS
C56	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C57	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C58	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C59	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C60	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C61	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C62	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C63	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C64	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C65	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C66	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C67	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C68	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C69	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C70	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C71	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C72	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C73	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C74	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C75	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C76	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C77	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C78	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C79	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C80	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C81	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C82	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C83	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C84	110172	CAP	ELECT	470 MFD	35 V			35VBSL470
C85	110172	CAP	ELECT	470 MFD	35 V			35VBSL470
C86	110174	CAP	ELECT	10,000 MFD	15 V			3050HS103U015 244G
C87	100126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C88	100126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C89	100126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C90	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C91	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C92	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C93	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C94	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C95	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C96	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C97	110140	CAP	CERAM	47 MFD	6 V	20%	05397	T368B685M006AS
C98	110140	CAP	CERAM	47 MFD	6 V	20%	05397	T368B685M006AS
C99	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	211083	DIODE	SILICO		1N916B		81349	1N916B
CR2	211083	DIODE	SILICO		1N916B		81349	1N916B
CR3	211083	DIODE	SILICO		1N916B		81349	1N916B
CR4	210004	DIODE	SILICO		1N4004		81349	1N4004
CR5	210004	DIODE	SILICO		1N4004		81349	1N4004
CR6	210004	DIODE	SILICO		1N4004		81349	1N4004
CR7	210004	DIODE	SILICO		1N4004		81349	1N4004
CR8	210070	DIODE	POWER		3 AMP		04713	MR501
CR9	210070	DIODE	POWER		3 AMP		04713	MR501
CR10	210070	DIODE	POWER		3 AMP		04713	MR501
CR11	210070	DIODE	POWER		3 AMP		04713	MR501
CR12	220026	DIODE	RF DET		1N82AG		81349	1N82AG
CR13	210004	DIODE	SILICO		1N4004		81349	1N4004
CR14	210004	DIODE	SILICO		1N4004		81349	1N4004
CR15	210004	DIODE	SILICO		1N4004		81349	1N4004
CR16	210004	DIODE	SILICO		1N4004		81349	1N4004
CR17	220034	DIODE	ZENER		1N960B		81349	1N960B
J4	600689	CONN		3 P			00779	4.583486-8
J8	920735	SOCKET	IC	16 P			71785	133-51-02-006
J9	920735	SOCKET	IC	16 P			71785	133-51-02-006
J10	920735	SOCKET	IC	16 P			71785	133-51-02-006

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
J14	600821	CONN		6 P			27264	09-03-1062
J15	600690	CONN		7 P			00779	4-583486-4
L1	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L2	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L3	310132	CHOKE	RF	.47 μH		10%	99800	1025-12
L4	310132	CHOKE	RF	.47 μH		10%	99800	1025-12
L5	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L6	310132	CHOKE	RF	.47 μH		10%	99800	1025-12
L7	310132	CHOKE	RF	.47 μH		10%	99800	1025-12
L8	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L9	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L10	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L11	310055	CHOKE	RF	4.7 μH			76493	9310-28
P5	600798	CONN	PLUG	3 P			27264	09-18-5031
Q1	200200	TRANS		NPN	200200		21793	200200
Q2	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q3	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q4	200068	TRANS	SILICO	PNP	2N4250		80131	2N4250
Q5	200068	TRANS	SILICO	PNP	2N4250		80131	2N4250
Q6	200200	TRANS		NPN	200200		21793	200200
Q7	200068	TRANS		PNP	2N4250		80131	2N4250
Q8	200068	TRANS		PNP	2N4250		80131	2N4250
Q9	200200	TRANS		NPN	200200		21793	200200
Q10	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q11	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q12	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q13	200068	TRANS		PNP	2N4250		80131	2N4250
Q14	200068	TRANS		PNP	2N4250		80131	2N4250
Q15	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q16	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q17	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q18	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q19	200099	TRANS	SILICO	PNP	2N4258		81349	2N4258
Q20	200099	TRANS	SILICO	PNP	2N4258		81349	2N4258
Q21	200099	TRANS	SILICO	PNP	2N4258		81349	2N4258
Q22	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q23	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q24	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q25	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q26	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q27	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q28	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q29	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
R1	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R2	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R3	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R4	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R5	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R6	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R7	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R8	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R9	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R10	000132	RES	CARBON	1.3 K		5% 1/4W	81349	RC07GF132J
R11	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R12	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R13	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R14	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R15	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R16	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R17	000132	RES	CARBON	1.3 K		5% 1/4W	81349	RC07GF132J
R18	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R19	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R20	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R21	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R22	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R23	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R24	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R25	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R26	000181	RES	CARBON	180 OHM		5% 1/4W	81349	RC07GF181J
R27	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R28	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R29	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R30	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R31	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R32	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R33	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R34	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R35	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R36	000361	RES	CARBON	360 OHM	5% 1/4W	81349	RC07GF361J
R37	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R38	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R39	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R40	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R41	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R42	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R43	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R44	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R45	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R46	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R47	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J
R48	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R49	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R50	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R51	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R52	000910	RES	CARBON	91 OHM	5% 1/4W	81349	RC07GF910J
R53	000910	RES	CARBON	91 OHM	5% 1/4W	81349	RC07GF910J
R54	040247	POT	CERMET	5 K	20% 1/2W	73138	72PX5K
R55	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R56	000431	RES	CARBON	430 OHM	5% 1/4W	81349	RC07GF431J
R57	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R58	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R59	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R60	000431	RES	CARBON	430 OHM	5% 1/4W	81349	RC07GF431J
R61	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R62	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R63	000431	RES	CARBON	430 OHM	5% 1/4W	81349	RC07GF431J
R64	000303	RES	CARBON	30 K	5% 1/4W	81349	RC07GF303J
R65	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R66	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R67	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R68	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R69	000303	RES	CARBON	30 K	5% 1/4W	81349	RC07GF303J
R70	000303	RES	CARBON	30 K	5% 1/4W	81349	RC07GF303J
R71	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R72	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R73	000512	RES	CARBON	5.2 K	5% 1/4W	81349	RC07GF512J
R74	000431	RES	CARBON	430 OHM	5% 1/4W	81349	RC07GF431J
R75	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R76	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R77	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R78	000112	RES	CARBON	1.1 K	5% 1/4W	81349	RC07GF112J
R79	000112	RES	CARBON	1.1 K	5% 1/4W	81349	RC07GF112J
R80	000112	RES	CARBON	1.1 K	5% 1/4W	81349	RC07GF112J
R81	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R82	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R83	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R84	000303	RES	CARBON	30 K	5% 1/4W	81349	RC07GF303J
R85	040247	POT	CERMET	5 K	20% 1/2W	73138	72PX5K
R86	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R87	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R88	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R89	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R90	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R91	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R92	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R93	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R94	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R95	000361	RES	CARBON	360 OHM	5% 1/4W	81349	RC07GF361J
R96	000910	RES	CARBON	91 OHM	5% 1/4W	81349	RC07GF910J
R97	000910	RES	CARBON	91 OHM	5% 1/4W	81349	RC07GF910J
R98	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R99	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R100	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R101	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R102	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R103	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R104	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R105	000361	RES	CARBON	360 OHM	5% 1/4W	81349	RC07GF361J
R106	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R107	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R108	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R109	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R110	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R111	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R112	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R113	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R114	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R115	000750	RES	CARBON	75 OHM	5% 1/4W	81349	RC07GF750J
R116	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R117	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R118	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J
R119	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R120	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J
R121	000621	RES	CARBON	620 OHM	5% 1/4W	81349	RC07GF621J
R122	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R123	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R124	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J
R125	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R126	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R127	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R128	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J
R129	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R130	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R131	000391	RES	CARBON	390 OHM	5% 1/4W	81349	RC07GF391J
R132	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R133	000131	RES	CARBON	130 OHM	5% 1/4W	81349	RC07GF131J
R134	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R135	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R136	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R137	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R138	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R139	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R140	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R141	000750	RES	CARBON	75 OHM	5% 1/4W	81349	RC07GF750J
R142	000161	RES	CARBON	160 OHM	5% 1/4W	81349	RC07GF161J
R143	001750	RES	CARBON	5.6 OHM	5% 1/4W	81349	RC07GF5R6J
R144	000391	RES	CARBON	390 OHM	5% 1/4W	81349	RC07GF391J
R145	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
S1	600604	SWITCH	PUSHBUTTON		2P2P	71590	PB15 Series
S2	600604	SWITCH	PUSHBUTTON		2P2P	71590	PB15 Series
S3	600915	SWITCH	ROTARY		3 Deck	11237	5P9028A
S4	600915	SWITCH	ROTARY		3 Deck	11237	5P9028A
S5	600920	SWITCH	SLIDE		2P3T	79727	GI-154/G-02-83-2/ G-20-18
S6	600919	SWITCH	SLIDE		2P2T	79727	GI-152/G-02-83-2/ G-20-18
U1	230360	IC			MM74C151N	27014	MM74C151N
U2	230234	IC			SN74LS04N	01295	SN74LS04N
U3	230330	IC			74SL367	01295	74LS367

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION		FSC	MANU P/N
U4	230193	IC	SN74LS00N	01295	SN74LS00N
U5	230202	IC	CA3102E	86884	CA3102E
U6	230202	IC	CA3102E	86884	CA3102E
U7	230314	IC	SN74LS75	01295	SN74LS75
U8	230317	IC	SN74LS90	01295	SN74LS90
U9	230374	IC	LS7031		LS7031
U10	230193	IC	SN74LS00N	01295	SN74LS00N
U11	230306	IC	SN74LS02	01295	SN74LS02
U12	230395	IC PROM "U 12"	HM-7603	34371	HM-7603
U13	230248	IC	SN74LS10N	01295	SN74LS10N
U14	230073	IC	7405	01295	7405
U15	320192	IC	SN74LS05N	01295	SN74LS05N
U16	230394	IC PROM "U 16"	HM-7603	34371	HM-7603
U17	230118	IC	CA3086	86884	CA3086
U18	230118	IC	CA3086	86884	CA3086
U19	230177	IC	SN74196	01295	SN74196
U20	230193	IC	SN74LS00N	01295	SN74LS00N
U21	230194	IC	SN74LS74N	01295	SN74LS74N
U22	230194	IC	SN74LS74N	01295	SN74LS74N
U23	230306	IC	SN74LS02	01295	SN74LS02
U24	230072	IC	7474	01295	7474
U25	230234	IC	SN74LS04N	01295	SN74LS04N
U26	230315	IC	SN74LS153N	01295	SN74LS153N
U27	230193	IC	SN74LS00N	01295	SN74LS00N
U29	230234	IC	SN74LS04N	01295	SN74LS04N
U30	230193	IC	SN74LS00N	01295	SN74LS00N
U31	230193	IC	SN74LS00N	01295	SN74LS00N
U32	230193	IC	SN74LS00N	01295	SN74LS00N
U33	230193	IC	SN74LS00N	01295	SN74LS00N
U34	230112	IC	MC10131	04713	MC10131
U35	230112	IC	MC10131	04713	MC10131
U36	230112	IC	MC10131	04713	MC10131
U37	230361	IC	MC10113P	04713	MC10113P
U38	230112	IC	MC10131	04713	MC10131
U39	230205	IC	MC10102P	04713	MC10102P
U40	230317	IC	SN74LS90	01295	SN74LS90
U41	230359	IC	DM74LS151N	27014	DM74LS151N
U42	230317	IC	SN74LS90	01295	SN74LS90
U43	230317	IC	SN74LS90	01295	SN74LS90
U44	230193	IC	SN74LS00N	01295	SN74LS00N
U45	230317	IC	SN74LS90	01295	SN74LS90

406869 – Assy., PCB, MOTHERBOARD continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
U46	230234	IC SN74LS04N	01295	SN74LS04N
U47	230306	IC SN74LS02	01295	SN74LS02
U48	230248	IC SN74LS10N	01295	SN74LS10N
U49	230205	IC MC10102P	04713	MC10102P
U50	230112	IC MC10131	04713	MC10131
U51	230362	IC MC10103P	04713	MC10103P
U52	230205	IC MC10102P	04713	MC10102P
U53	230205	IC MC10102P	04713	MC10102P
U54	230362	IC MC10103P	04713	MC10103P
U55	230317	IC SN74LS90	01295	SN74LS90
U56	230317	IC SN74LS90	01295	SN74LS90
U57	230317	IC SN74LS90	01295	SN74LS90
U58	230317	IC SN74LS90	01295	SN74LS90
U59	230194	IC SN74LS74N	01295	SN74LS74N
U60	230346	IC 74LS157	01295	74LS157
U61	230112	IC MC10131	04713	MC10131
U62	230205	IC MC10102P	04713	MC10102P
U63	230234	IC SN74LS04N	01295	SN74LS04N
W1	600245	JUMPER INSULATED		L-2007-1LP
Y1	730655	OSCILLATOR TXCO	21793	730655
Z1	080020	RES CERMET 10 K Network 8P.7R 2%	11236	750-81-R10KΩ
Z2	080011	RES CERMET 1 K Network 8P.7R 2%	11236	750-81-R1KΩ
Z3	080021	RES CERMET 510 OHM Network 14P.13R 2%	11236	760-1-R5KΩ
Z4	080020	RES CERMET 10 K Network 8P.7R 2%	11236	750-81-R10KΩ
Z5	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z6	080010	RES CERMET TTL-ECL Network	11236	761-45
Z7	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z8	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z9	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z10	080010	RES CERMET TTL-ECL Network	11236	761-45
Z11	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z12	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z13	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z14	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z15	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω
Z16	080010	RES CERMET TTL-ECL Network	11236	761-45
Z17	080002	RES CERMET 500 OHM Network 8P.7R 2%	11236	750-81-R500Ω

406863 – Assy., PCB, DISPLAY

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR2	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR3	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR4	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR5	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR6	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR7	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR8	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR9	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR10	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR11	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR12	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR13	211083	DIODE	SILICO		1N916B		81349	1N916B
CR14	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
LED1	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED2	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED3	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED4	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED5	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED6	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED7	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED8	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
LED9	210072	DIODE	LED LAMP, YELLOW				50434	HP5082-4550
Q1	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q2	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q3	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q4	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q5	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q6	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q7	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q8	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
Q9	200251	TRANS	SILICO	NPN	MPS-A12		04713	MPS-A12
R1	040302	POT	SWITCH	1 M/SPST			71450	055-T200-D
R2	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J

406863 – Assy., PCB, DISPLAY continued

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R3	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J
R4	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J
R5	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J
R6	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J
R7	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J
R8	000150	RES	CARBON	15 OHMS	5%	1/4W	81349	RC07GF150J
R9	000221	RES	CARBON	220 OHMS	5%	1/4W	81349	RC07GF221J
R10	000100	RES	CARBON	10 OHMS	5%	1/4W	81349	RC07GF100J
S1	040302	POT	SWITCH	PART OF 040302 (R1)				
Z1	080022	RES	CERMET	220 OHMS	- Network	14P.7R 2%	11236	760-3-R220Ω

406879 – Assy., PCB, SWITCHING

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C7	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C8	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C10	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TC-DI-1(N750)
C11	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TC-DI-1(N750)
C12	100016	CAP	CERAM	27 PFD	1000 V	10%	71590	DD270
C13	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C15	101174	CAP	CERAM	.01 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C16	100016	CAP	CERAM	27 PFD	1000 V	10%	71590	DD270
C17	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C18	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C20	100102	CAP	CERAM	47 PFD	1000 V	5%	56289	C030B102H470J
C21	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TC-DI-1(N750)
C22	100102	CAP	CERAM	47 PFD	1000 V	5%	56289	C030B102H470J
C23	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TC-DI-1(N750)
C24	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C25	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR2	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR4	211236	DIODE	SILICO		007		21793	211236
CR5	211236	DIODE	SILICO		007		21793	211236
CR6	220031	DIODE	SILICO, ZENER		3.3 V		04713	1/4M3.3AZ5
CR7	220031	DIODE	SILICO, ZENER		3.3 V		04713	1/4M3.3AZ5
CR8	220031	DIODE	SILICO, ZENER		3.3 V		04713	1/4M3.3AZ5
CR9	220031	DIODE	SILICO, ZENER		3.3 V		04713	1/4M3.3AZ5
CR10	211236	DIODE	SILICO		007		21793	211236
CR11	211236	DIODE	SILICO		007		21793	211236
J2	600671	CONN	6 P				71785	252-06-30-160
J6	600914	CONN	HOUSING, Single Row, 3 Contrast				00779	87175-8
J7	600914	CONN	HOUSING, Single Row, 3 Contrast				00779	87175-8
J101	600567	CONN	RECPTLE				02660	31-236
J102	600567	CONN	RECPTLE				02660	31-236

406879 – Assy., PCB, SWITCHING continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q1	200219	TRANS Matched Pair (2N3563) (W/Q2)	21793	200019
Q2	200219	TRANS Matched Pair (2N3563) (W/Q1)	21793	200019
Q3	200241	TRANS FET, Matched Dual Chan	17856	E420
Q4	200241	TRANS FET, Matched Dual Chan	17856	E420
Q5	200219	TRANS Matched Pair (2N3563) (W/Q6)	21793	200219
Q6	200219	TRANS Matched Pair (2N3563) (W/Q5)	21793	200219
R1	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R2	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R3	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R4	010872	RES METAL 1.54 K 1% 1/10W	81349	RN55C1541F
R5	040187	POT CERMET 500 OHM 20% 3/4W	11237	360T501B
R6	000681	RES CARBON 680 OHM 5% 1/4W	81349	RC07GF681J
R7	040303	POT SWITCH 25K/SPST	71450	055-U200-D
R8	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R9	010399	RES METAL 900 K .1% 1/8W	81349	RN609003B
R10	010399	RES METAL 900 K .1% 1/8W	81349	RN609003B
R11	000434	RES CARBON 430 K 5% 1/4W	81349	RC07GF434J
R12	000681	RES CARBON 680 OHM 5% 1/4W	81349	RC07GF681J
R13	040303	POT SWITCH 25K/SPST	71450	055-U200-D
R14	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R15	010872	RES METAL 1.54 K 1% 1/10W	81349	RN55C1541F
R16	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R17	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R18	040187	POT CERMET 500 OHM 20% 3/4W	11237	360T501B
R19	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R20	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R21	000434	RES CARBON 430 K 5% 1/4W	81349	RC07GF434J
R22	010872	RES METAL 1.54 K 1% 1/10W	81349	RN55C1541F
R23	010872	RES METAL 1.54 K 1% 1/10W	81349	RN55C1541F
R24	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R25	010680	RES METAL 90.9 K 1% 1/10W	81349	RN55C9092F
R26	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R27	010680	RES METAL 90.9 K 1% 1/10W	81349	RN55C9092F
R28	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R29	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R30	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R31	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R32	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R33	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J

406879 – Assy., PCB, SWITCHING continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
S1	600916	SWITCH SLIDE 2P2T	79727	GF-126/G-02-30-3/ G-20-39
S2	600916	SWITCH SLIDE 2P2T	79727	GF-126/G-02-30-3/ G-20-39
S3	600917	SWITCH SLIDE 2P3T	79727	G-128L/G-02-30-3/ G-20-39
S4	600916	SWITCH SLIDE 2P2T	79727	GF-126/G-02-30-3/ G-20-39
S5	600916	SWITCH SLIDE 2P2T	79727	GF-126/G-02-30-3/ G-20-39
S6	040303	POT SWITCH PART OF R7		
S7	600917	SWITCH SLIDE 2P3T	79727	G-128L/G-02-30-3/ G-20-39
S8	600917	SWITCH SLIDE 2P3T	79727	G-128L/G-02-30-3/ G-20-39
S9	040303	POT SWITCH PART OF R13		

406865 – Assy., PCB, SWITCHING

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR2	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR3	211083	DIODE	SILICO		1N916B		81349	1N916B
CR4	211083	DIODE	SILICO		1N916B		81349	1N916B
CR5	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR6	211083	DIODE	SILICO		1N916B		81349	1N916B
CR7	211083	DIODE	SILICO		1N916B		81349	1N916B
CR8	211083	DIODE	SILICO		1N916B		81349	1N916B
CR9	211083	DIODE	SILICO		1N916B		81349	1N916B
CR10	211083	DIODE	SILICO		1N916B		81349	1N916B
CR11	211083	DIODE	SILICO		1N916B		81349	1N916B
CR12	211083	DIODE	SILICO		1N916B		81349	1N916B
CR13	211083	DIODE	SILICO		1N916B		81349	1N916B
J2	600671	CONN		6 P			71785	252-06-30-160
J3	600670	CONN		10 P			71785	252-10-30-160
J101	600567	CONN	RECPTLE				02660	31-236
J102	600567	CONN	RECPTLE				02660	31-236
R1	000681	RES	CARBON	680 OHMS		5% 1/4W	81349	RC07GF681J
R2	000681	RES	CARBON	680 OHMS		5% 1/4W	81349	RC07GF681J
R3	000242	RES	CARBON	2.4 K		5% 1/4W	81349	RC07GF242J
R4	040303	POT	SWITCH	1 M/SPST			71450	055-T200-D
R5	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R6	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R7	040303	POT	SWITCH	1 M/SPST			71450	055-T200-D
R8	000242	RES	CARBON	2.4 K		5% 1/4W	81349	RC07GF242J
S1	600916	SWITCH	SLIDE	2P2T			79727	GF-126/G-02-30-3/ G-20-39
S2	600916	SWITCH	SLIDE	2P2T			79727	GF-126/G-02-30-3/ G-20-39
S3	600917	SWITCH	SLIDE	2P3T			79727	G-128L/G-02-30-3/ G-20-39
S4	600916	SWITCH	SLIDE	2P2T			79727	GF-126/G-02-30-3/ G-20-39

406865 – Assy., PCB, SWITCHING continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
S5	600916	SWITCH SLIDE 2P2T	79727	GF-126/G-02-30-3/ G-20-39
S6	040303	POT SWITCH PART OF R4		
S7	600918	SWITCH SLIDE 2P4T	79727	G-141-S-G-02-30-3/ G-20-39
S8	600918	SWITCH SLIDE 2P4T	79727	G-141-S-G-02-30-3/ G-20-39
S9	040303	POT SWITCH PART OF R7		
Z1	080020	RES CERMET 10 K Network 8P.7R 2%	11236	750-81-R10KΩ

406868 – Assy., PCB, IEEE-488/1975 INTERFACE

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C5	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C6	100084	CAP	CERAM	1.5 ± .5 PFD	1000 V		56289	C030B102S1R5D
C7	100084	CAP	CERAM	1.5 ± .5 PFD	1000 V	5%	56289	C030B102S1R5D
C8	100119	CAP	CERAM	470 PFD	100 V	5%	72982	8121M100-C0G-471J
C9	100123	CAP	CERAM	3.0 ± .5 PFD	1000 V		52689	C030B102S3R0D
C10	100119	CAP	CERAM	470 PFD	100 V	5%	72982	8121-M100-C0G-471J
C11	100123	CAP	CERAM	3.0 ± .5 PFD	1000 V		56289	C030B102S3R0D
C12	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C15	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C16	100081	CAP	CERAM	4.7 PFD	1000 V	5%	56289	C030B102E4R7D
C17	100081	CAP	CERAM	4.7 PFD	1000 V	5%	56289	C030B102E4R7D
C18	100102	CAP	CERAM	47 PFD	1000 V	5%	56289	C030B102H470J
C19	100095	CAP	CERAM	2.7 ± .5 PFD	1000 V		56289	C030B102S2R7D
C20	100102	CAP	CERAM	47 PFD	1000 V	5%	56289	C030B102H470J
C21	100095	CAP	CERAM	2.7 ± .5 PFD	1000 V		56289	C030B102S2R7D
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C23	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C24	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C25	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C26	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C27	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C28	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C29	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C30	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C31	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C32	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C33	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C34	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C35	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C36	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C37	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C38	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C39	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C40	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M

406868 – Assy., PCB, IEEE-488/1975 INTERFACE continued

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C41	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C42	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C43	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C44	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C45	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C46	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C47	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C48	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C49	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C50	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C51	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C52	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C53	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C54	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C55	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C56	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C57	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C58	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C59	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C60	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C61	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C62	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C63	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C64	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C65	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C66	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C67	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C68	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C69	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C70	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
CR1	211083	DIODE	SILICO		1N916B		81349	1N916B
CR2	211083	DIODE	SILICO		1N916B		81349	1N916B
CR3	211083	DIODE	SILICO		1N916B		81349	1N916B
CR4	211083	DIODE	SILICO		1N916B		81349	1N916B
CR5	211083	DIODE	SILICO		1N916B		81349	1N916B
CR6	211083	DIODE	SILICO		1N916B		81349	1N916B
CR7	211083	DIODE	SILICO		1N916B		81349	1N916B
CR8	211083	DIODE	SILICO		1N916B		81349	1N916B
CR9	211083	DIODE	SILICO		1N916B		81349	1N916B
CR10	211083	DIODE	SILICO		1N916B		81349	1N916B

406868 – Assy., PCB, IEEE-488/1975 INTERFACE continued

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
CR11	211083	DIODE	SILICO		1N916B	81349	1N916B
CR12	220031	DIODE	SILICO, ZENER		3.3 V	04713	1/4M3.3AZ5
CR13	220031	DIODE	SILICO, ZENER		3.3 V	04713	1/4M3.3AZ5
CR14	220031	DIODE	SILICO, ZENER		3.3 V	04713	1/4M3.3AZ5
CR15	220031	DIODE	SILICO, ZENER		3.3 V	04713	1/4M3.3AZ5
CR16	220031	DIODE	SILICO, ZENER		3.3 V	04713	1/4M3.3AZ5
CR17	210036	DIODE			FD300	07263	FD300
CR18	210036	DIODE			FD300	07263	FD300
CR19	210036	DIODE			FD300	07263	FD300
CR20	210036	DIODE			FD300	07263	FD300
CR21	211083	DIODE	SILICO		1N916B	81349	1N916B
CR22	210014	DIODE			1N4005	81349	1N4005
J6	600914	CONN	HOUSING	SINGLE ROW, 3 CONTACT		00779	87175-8
J7	600914	CON	HOUSING	SINGLE ROW, 3 CONTACT		00779	87175-8
J8	920735	SOCKET, IC		16 PIN		71785	133-51-02-006
J9	920735	SOCKET, IC		16 PIN		71785	133-51-02-006
J10	920735	SOCKET, IC		16 PIN		71785	133-51-02-006
J11	600227	CONN		18 PIN		71785	251-18-30-160
K1	310125	RELAY	REED	1 FORM A	5 V	21793	310125
K2	310127	RELAY	REED			15636	R-6370-1
K3	310125	RELAY	REED	1 FORM A	5 V	21793	310125
K4	310127	RELAY	REED			15636	R-6370-1
K5	310127	RELAY	REED			15636	R-6370-1
K6	310127	RELAY	REED			15636	R-6370-1
K7	310127	RELAY	REED			15636	R-6370-1
K8	310127	RELAY	REED			15636	R-6370-1
K9	310127	RELAY	REED			15636	R-6370-1
K10	310127	RELAY	REED			15636	R-6370-1
K11	310127	RELAY	REED			15636	R-6370-1
L1	310068	CHOKE	RF	1 μH	10%	99800	1537-12
L2	310068	CHOKE	RF	1 μH	10%	99800	1537-12
Q1	200200	TRANS		NPN	200200	21793	200200
Q2	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248
Q3	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248
Q4	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248
Q5	200200	TRANS		NPN	200200	21793	200200
Q6	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248

406868 – Assy., PCB, IEEE-488/1975 INTERFACE continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q7	200241	TRANS FET Matched Dual Chan	17856	E4200
Q8	200241	TRANS FET Matched Dual Chan	17856	E4200
Q9	200219	TRANS MATCHED PAIR (2N3563) W/Q10	21793	200219
Q10	200219	TRANS MATCHED PAIR (2N3563) W/Q9	21793	200219
Q11	200219	TRANS MATCHED PAIR (2N3563) W/Q12	21793	200219
Q12	200219	TRANS MATCHED PAIR (2N3563) W/Q11	21793	200219
Q13	200037	TRANS SILICO NPN 2N3646	80131	2N3646
R1	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R2	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R3	000513	RES CARBON 51 K 5% 1/4W	81349	RC07GF513J
R4	010991	RES METAL 990 K .1% 1/4W	81349	RN65C9903B
R5	010991	RES METAL 990 K .1% 1/4W	81349	RN65C9903B
R6	000392	RES CARBON 3.9 K 5% 1/4W	81349	RC07GF392J
R7	010988	RES METAL 10.1 K .1% 1/10W	81349	RN55C1012B
R8	010988	RES METAL 10.1 K .1% 1/10W	81349	RN55C1012B
R9	000392	RES CARBON 3.9 K 5% 1/4W	81349	RC07GF392J
R10	012004	RES METAL 4.12 K 1% 1/10W	81349	RN55C4121F
R11	000392	RES CARBON 3.9 K 5% 1/4W	81349	RC07GF392J
R12	000162	RES CARBON 1.6 K 5% 1/4W	81349	RC07GF162J
R13	010873	RES METAL 2.21 K 1% 1/10W	81349	RN55C2211F
R14	010969	RES METAL 1.62 K 1% 1/10W	81349	RN55C1621F
R15	010873	RES METAL 2.21 K 1% 1/10W	81349	RN55C2211F
R16	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R17	000200	RES CARBON 20 OHM 5% 1/4W	81349	RC07GF200J
R18	010990	RES METAL 900 K .1% 1/4W	81349	RN65C9003B
R19	010990	RES METAL 900 K .1% 1/4W	81349	RN65C9003B
R20	010989	RES METAL 111 K .1% 1/10W	81349	RN55C1113B
R21	010989	RES METAL 111 K .1% 1/10W	81349	RN55C1113B
R22	000162	RES CARBON 1.6 K 5% 1/4W	81349	RC07GF162J
R23	010969	RES METAL 1.62 K 1% 1/10W	81349	RN55C1621F
R24	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R25	010988	RES METAL 10.1 K .1% 1/10W	81349	RN55C1012B
R26	000392	RES CARBON 3.9 K 5% 1/4W	81349	RC07GF132J
R27	000434	RES CARBON 430 K 5% 1/4W	81349	RC07GF434J
R28	000434	RES CARBON 430 K 5% 1/4W	81349	RC07GF434J
R29	000392	RES CARBON 3.9 K 5% 1/4W	81349	RC07GF392J
R30	012004	RES METAL 4.12 K 1% 1/10W	81349	RN55C4121F
R31	000162	RES CARBON 1.6 K 5% 1/4W	81349	RC07GF162J
R32	010879	RES METAL 1 M 1% 1/10W	81349	RN55D1004F
R33	010879	RES METAL 1 M 1% 1/10W	81349	RN55D1004F

406868 – Assy., PCB, IEEE-488/1975 INTERFACE continued

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R34	000392	RES	CARBON	3.9 K	5% 1/4W	81349	RC07GF392J
R35	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R36	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R37	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R38	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R39	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R40	000513	RES	CARBON	51 K	5% 1/4W	81349	RC07GF513J
R41	040187	POT	CERMET	500 OHM	20% 3/4W	11237	360T501B
R42	040187	POT	CERMET	500 OHM	20% 3/4W	11237	360T501B
R43	040187	POT	CERMET	500 OHM	20% 3/4W	11237	360T501B
R44	040187	POT	CERMET	500 OHM	20% 3/4W	11237	360T501B
R45	000162	RES	CARBON	1.6 K	5% 1/4W	81349	RC07GF162J
R46	012003	RES	METAL	1.91 K	1% 1/10W	81349	RN55C1911F
R47	012003	RES	METAL	1.91 K	1% 1/10W	81349	RN55C1911F
R48	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R49	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R50	010705	RES	METAL	4.53 K	1% 1/10W	81349	RN55C4531F
R51	010705	RES	METAL	4.53 K	1% 1/10W	81349	RN55C4531F
R52	010705	RES	METAL	4.53 K	1% 1/10W	81349	RN55C4531F
R53	010705	RES	METAL	4.53 K	1% 1/10W	81349	RN55C4531F
R54	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R55	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R56	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R57	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R58	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R59	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R60	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R61	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R62	010872	RES	METAL	1.54 K	1% 1/10W	81349	RN55C1541F
R63	010872	RES	METAL	1.54 K	1% 1/10W	81349	RN55C1541F
R64	040187	POT	CERMET	500 OHM	20% 3/4W	11237	360T501B
R65	040187	POT	CERMET	500 OHM	20% 3/4W	11237	360T501B
R66	010872	RES	METAL	1.54 K	1% 1/10W	81349	RN55C1541F
R67	010872	RES	METAL	1.54 K	1% 1/10W	81349	RN55C1541F
R68	000621	RES	CARBON	620 OHM	5% 1/4W	81349	RC07GF621J
R69	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R70	000621	RES	CARBON	620 OHM	5% 1/4W	81349	RC07GF621J
R71	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R72	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R73	000392	RES	CARBON	3.9 K	5% 1/4W	81349	RC07GF392J
R74	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J

406868 – Assy., PCB, IEEE-488/1975 INTERFACE continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R75	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
S1	600926	SWITCH PUSHBUTTON, Momentary Single 2 Pole	71590	PBI Series
S2	600926	SWITCH PUSHBUTTON, Momentary Single 2 Pole	71590	PBI Series
U1	230193	IC SN74LS00N	01295	SN74LS00N
U2	230193	IC SN74LS00N	01295	SN74LS00N
U3	230207	IC MC1408L-8	04713	MC1408L-8
U4	230238	IC 74LS164	27014	74LS164
U5	230073	IC 7405	01295	7405
U6	230073	IC 7405	01295	7405
U7	230190	IC LM324	27014	LM324
U8	230194	IC SN74LS74N	01295	SN74LS74N
U9	230238	IC 74LS164	27014	74LS164
U10	230207	IC MC1408L-8	04713	MC1408L-8
U11	230118	IC CA3086	86884	CA3086
U12	230330	IC 74LS367	01295	74LS367
U13	230371	IC 4053BN	27014	4053BN
U14	230330	IC 74LS367	01295	74LS367
U15	230330	IC 74LS367	01295	74LS367
U16	230330	IC 74LS367	01295	74LS367
U17	230368	IC 74LS138	27014	74LS138
U18	230368	IC 74LS138	27014	74LS138
U19	230248	IC SN74LS10N	01295	SN74LS10N
U20	230238	IC 74LS164	27014	74LS164
U21	230330	IC 74LS367	01295	74LS367
U22	230370	IC 2716	34649	2716
U23	230366	IC DM74LS174N	27014	DM74LS174N
U24	230194	IC SN74LS74N	01295	SN74LS74N
U25	230193	IC SN74LS00N	01295	SN74LS00N
U26	230234	IC SN74LS04N	01295	SN74LS04N
U27	230366	IC DM74LS174N	27014	DM74LS174N
U28	230356	IC 74LS175	27014	74LS175
U29	230234	IC SN74LS04N	01295	SN74LS04N
U30	230238	IC 74LS164	27014	74LS164
U31	230330	IC 74LS367	01295	74LS367
U32	230237	IC SN74LS123N	01295	SN74LS123N
U33	230369	6802-P	04713	6802-P
U34	230330	74LS367	01295	74LS367
U35	230330	74LS367	01295	74LS367
U36	230356	74LS175	27014	74LS175

406868 – Assy., PCB, IEEE-488/1975 INTERFACE continued

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
U37	230356	74LS175	27014	74LS175
U38	230330	74LS367	01295	74LS367
U40	230367	74LS93	27014	74LS93
U41	230330	74LS367	01295	74LS367
U42	230194	SN74LS74N	01295	SN74LS74N
U43	230237	SN74LS123N	01295	SN74LS123N
U44	230194	SN74LS74N	01295	SN74LS74N
U45	230275	MC7805CT	04713	MC7805CT
U46	230234	SN74LS04N	01295	SN74LS04N
W1	600245	JUMPER INSULATED		L-2007-1LP
W2	600245	JUMPER INSULATED		L-2007-1LP
Z1	080020	RES CERMET 10 K Network 8P.7R 2%	11236	750-81-R10KΩ

406867 – Assy., PCB, I/O BUFFER

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C-1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
U1	230246	IC			MC3440P		04713	MC3440P
U2	230246	IC			MC3440P		04713	MC3440P
U3	230246	IC			MC3440P		04713	MC3440P
U4	230246	IC			MC3440P		04713	MC3440P
Z1	080020	RES	CERMET	10 K	Network	8P,7R 2%	11236	750-81-R10KΩ

406900 – Assy., REAR INPUT, OPTION 01

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
J16	600610	CONN RECPTLE	98291	50-053-0000
J17	600610	CONN RECPTLE	98291	50-053-0000
J204	600808	CONN BNC	02660	31-010
J206	600931	CONN RF BNC TO SMC, Fused	16733	701938-002
J207	600808	CONN BNC	02660	31-010
P16	600483	CONN COAX, Plug	02660	27-7
P17	600483	CONN COAX, Plug	02660	27-7

406881 – Assy., PCB, REFERENCE MULTIPLIER

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C5	100053	CAP	CERAM	56 PFD	1000 V	5%	56289	C030A102J560J
C6	100018	CAP	CERAM	120 PFD	500 V	10%	71471	ETCD(N5600)
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C8	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C10	100018	CAP	CERAM	120 PFD	500 V	10%	71471	ETCD(N5600)
C11	100050	CAP	CERAM	2.2 PFD	1000 V	5%	56289	C030B102S2R2D
C12	100051	CAP	CERAM	3 PFD	500 V		71471	TCD-B1-0
C13	100097	CAP	CERAM	12 PFD	1000 V	5%	56289	C030B102E120J
C14	100064	CAP	CERAM	390 PFD	1000 V	10%	71590	DD391
CR1	211083	DIODE	SILICO		1N916B		81349	1N916B
CR2	211083	DIODE	SILICO		1N916B		81349	1N916B
CR3	211083	DIODE	SILICO		1N916B		81349	1N916B
CR4	211083	DIODE	SILICO		1N916B		81349	1N916B
CR5	211083	DIODE	SILICO		1N916B		81349	1N916B
L1	310072	CHOKE	RF	2.2 μH		10%	99800	1537-20
Q1	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q2	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q3	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q4	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
R1	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R2	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R3	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R4	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R5	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R6	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R7	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R8	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R9	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R10	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R11	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R12	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
Y1	920583	CRYSTAL		9.9988 MHz	H33 Holder		21793	920583

406912 – Assy., AUTO TRIGGER, 40 Hz, OPTION 12

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R74	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J

406818 – Assy., OSCILLATOR, OPTION 22

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
P11	600797	CONN	RECEPTLE	3 PIN			27264	03-09-1032

406819 – Assy., OSCILLATOR, OPTION 24

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
P11	600797	CONN	RECEPTLE	3 PIN			27264	03-09-1032

406918 – Assy., PCB, POWER SUPPLY, OVEN OSCILLATOR

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368B685M035AS
C2	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368B685M035AS
C3	110180	CAP	ELECT	1300 MFD	50 V	10%	80031	ME3050GL132U050
CR1	210004	DIODE	SILICO		1N4004		81349	1N4004
CR2	210004	DIODE	SILICO		1N4004		81349	1N4004
CR3	210004	DIODE	SILICO		1N4004		81349	1N4004
CR4	21004	DIODE	SILICO		1N4004		81349	1N4004
J21	600798	CONN	PLUG	3 P			27264	09-18-5031
R1	001259	RES	CARBON	2.4 K		5% 1/2W	81349	RC20GF242J
R2	040259	RES	CARBON	200 OHM		20% 1/2W	73138	72XW200
R3	000121	RES	CARBON	120 OHM		5% 1/4W	81349	RC07GF120J
S1	600521	SWITCH		DPDT			82389	46256LFE
T1	730682	TRANSFORMER		115V - 230V			21793	730682
U1	230271	IC			LM340-24		27014	LM340-24

406904 – Assy., CABLE, AC POWER

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
P21-1	600650	TERMINAL PIN Female	27264	1433
P21-3	600651	TERMINAL PIN Male	27264	1434
P21	600797	CONN RECPTLE 3 P	27264	03-09-1032

406897 – Assy., R.F., 512 MHz

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
F101	920814	FUSE RF 1/8 AMP	16733	913451-001
J101	600931	CONN RF BNC TO SMC, Fused	16733	701938-002

406907 – Assy., PCB, R.F., 512 MHz

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	100106	CAP	CERAM	100 PFD	1000 V	10%	56289	10-TS-T10
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C8	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C9	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C11	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C12	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C13	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C14	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C15	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C16	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C17	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
CR1	220007	DIODE	SILICO, ZENER		1N751A		81349	1N751A
CR2	210026	DIODE	RF, DET		1N82AG		81349	1N82AG
CR3	210089	DIODE	LOW OFF SET, Schottky		HP5082-2835		50434	HP5082-2835
CR4	210089	DIODE	LOW OFF SET, Schottky		HP5082-2835		50434	HP5082-2835
CR5	210089	DIODE	LOW OFF SET, Schottky		HP5082-2835		50434	HP5082-2835
CR6	210089	DIODE	LOW OFF SET, Schottky		HP5082-2835		50434	HP5082-2835
CR7	210089	DIODE	LOW OFF SET, Schottky		HP5082-2835		50434	HP5082-2835
CR8	210089	DIODE	LOW OFF SET, Schottky		HP5082-2835		50434	HP5082-2835
L1	310051	CHOKE		1.0 μH			83125	DD1.00
Q1	200200	TRANS		NPN			21793	200200
Q2	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q3	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q4	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248

406907 – Assy., PCB, R.F., 512 MHz continued

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q5	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q6	200194	TRANS	SILICO	NPN	2N5179		81349	2N5179
Q7	200194	TRANS	SILICO	NPN	2N5179		81349	2N5179
Q8	200194	TRANS	SILICO	NPN	2N5179		81349	2N5179
Q10	200200	TRANS		NPN			21793	200200
R1	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R2	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R3	000511	RES	CARBON	511 OHM		5% 1/4W	81349	RC07GF511J
R4	000511	RES	CARBON	511 OHM		5% 1/4W	81349	RC07GF511J
R5	000511	RES	CARBON	511 OHM		5% 1/4W	81349	RC07GF511J
R6	000511	RES	CARBON	511 OHM		5% 1/4W	81349	RC07GF511J
R7	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R9	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R10	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R11	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R14	000303	RES	CARBON	30 K		5% 1/4W	81349	RC07GF303J
R15	000182	RES	CARBON	1.8 K		5% 1/4W	81349	RC07GF182J
R16	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R17	000560	RES	CARBON	56 OHM		5% 1/4W	81349	RC07GF560J
R18	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R19	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF361J
R20	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R21	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R22	000242	RES	CARBON	2.4 K		5% 1/4W	81349	RC07GF242J
R23	001743	RES	CARBON	51 OHM		5% 1/2W	81349	RC20GF510J
R24	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R25	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R26	000623	RES	CARBON	62 K		5% 1/4W	81349	RC07GF623J
R27	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R28	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R29	000103	RES	CARBON	1 K		5% 1/4W	81349	RC07GF103J
U1	230362	IC			MC10103P		047B	MC10103P
U2	230307	IC			LM311H		27014	LM311H
U3	230390	IC			SP8635B		52648	SP8635B
U4	230391	IC	Amplifier		GPD-401		24539	GPD-401
U5	230392	IC	Amplifier		GPD-402		24539	GPD-402
U6	230392	IC	Amplifier		GPD-402		24539	GPD-402
Z1	080025	RES	CERMET	2 K	Network	6P5R 2%	11236	750-61-R2KΩ
Z2	080024	RES	CERMET	3.3 K	Network	6P5R 2%	11236	750-61-R3.3KΩ

406911 – Assy., EXTENDED PROGRAMMING, OPTION 55E

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
CR23	211083	DIODE	SILICO		1N916B		81349	1N916B
C24	211083	DIODE	SILICO		1N916B		81349	1N916B
K12	310125	RELAY	REED	1 Form A	5 V		21793	310125
K13	310125	RELAY	REED	1 Form A	5 V		21793	310125
R76	001743	RES	CARBON	51 OHM		5% 1/2W	81349	RC20GF510J
R77	001743	RES	CARBON	51 OHM		5% 1/2W	81349	RC20GF510J
U22	230413	IC			MM52132N		27014	MM52132N